Department of Electrical and Computer Engineering

High Speed Audio to Universal Serial Bus Interface

By

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Bachelor of Technology
(Electrical Engineering)

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TITLE: High Speed Audio to Universal Serial Bus Interface

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ABSTRACT

Curtin University of Technology has a large amount of audio files stored on tapes and audiocassette's. The content of these archives is, by and large, speech. The primary purpose of this audio digitisation project is preservation and play back of the legacy audio contents on ether a MAC or Windows based machine.

The high speed digitisation process, obviously, is not a simple one and it poses a number of challenges that needs to be address. Some of those challenges are due to the variety of original media, media quality and original recording quality. Other concerns include the choice of the digital file format, the storage medium, as well as the choice of appropriate hardware, software, compression and digitisation procedures. Even with all these challengers, there are many benefits of digitising audio recordings. These include the contents of the audio recordings to be preserved without loss of quality as well as the transmission of the audio file over many different digital mediums such as computer networks, wireless networks or the internet.

INDEXING TERMS

	GOOD	AVERAGE	POOR
TECHNICAL WORK			
REPORT PRESENTATION			

CO-EXAMINER

EXAMINER

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20th May 2006

Dear Sir,

I am pleased to be able to submit this thesis titled 'High Speed Audio to Universal Serial Bus Interface' as part of the requirements of the Bachelor of Technology Computer System and Networking degree. To the best of my knowledge this thesis contains no material previously published by another person except where due reference is made.

Yours sincerely,

Simon Dunn (12561010)

ACKNOWLEDGMENTS

I would like to thank all of the teaching staff for their guidance through this course with a special thanks to Iain Murray and Alex Wong for their patience and guidance throughout this project and associated units and my partner Kerry Ferguson for he input and guidance.

NOMENCLATURE

AC	-	Alternating Current
ACK	-	Acknowledgment
ADC	-	Analogue to Digital Converter
AM	-	Amplitude Modulation
ASCII	-	American Standard Code
Binary	-	Base two number made up from ones and zero
C	-	Capacitor Electrical Component
CD	-	Compact Disc
CMOS	-	Complementary Metal Oxide Semiconductor
CRC	-	Cyclic Redundancy Checking
CS	-	Chip Select
dB	-	Decibel Measurement of Power and Sound
D0 –D7	-	Data bus made up of eight lines
DC	-	Direct Current
DIL	-	Dual in Line Layout of Integrated Circuit
ECS	-	EPROM Chip Select
ECLK	-	EPROM Clock
EDAT	-	EPROM DATA
EF	-	Empty Flag Pin on Integrated Circuit
FIFO	-	First in First Out
FM	-	Frequency Modulation
GND	-	Ground Electrical Potential
Hertz	-	Cycles Per Second
IC	-	Integrated Circuit

I/O	-	Input / Output Pin on Integrated Circuit
ISR	-	Integrating Switching Regulator
Kbyte	-	Thousands of 8-Bit Binary Number
KHz	-	Thousands of Cycles Per Second
MAC	-	Type of operating system manufactured by Apple
MByte	-	Millions 8-Bit Binary Number
MHz	-	Millions of Cycles Per Second
MP3	-	A New Standard for Audio Compression
MPEG	-	Moving Picture Experts Group
mV	-	MilliVolt $1x10^{-3}$ Volts
NAK	-	No Acknowledgment
NRZI	-	Non-Return to Zero Inverted Transmission Protocol
ns	-	Nano seconds $1x10^{-9}$ seconds
Π	-	Mathematical Symbol for Pie (3.141)
P	-	Pot Variable Resistor
PCB	-	Printed Circuit Board
PEN	-	Power Enable
Pk – Pk	-	Peak to Peak Measurement Between to Point
PWR	-	Power
Q0-Q8	-	Data Bus made up of Eight Lines
R	-	Resistor Electrical Component
RAM	-	Random Access Memory
RD	-	Read Pin on Integrated Circuit
RDY	-	Ready Pin on Integrated Circuit
RSTI	-	Reset Input Pin on Integrated Circuit

RSTO	-	Reset Output Pin on Integrated Circuit
RXF	-	Receive Flap pin on Integrated Circuit
SIE	-	Serial Interface Engine
SI/W	-	Send Immediate / Wake Up Pin on Integrated Circuit
SPS	-	Sample Per Second
TTL	-	Transistor, Transistor Logic
TXE	-	Transmit Pin on Integrated Circuit
USB	-	Universal Serial Bus
V	-	Voltage
Vin	-	Voltage Input
Vo	-	Voltage Output
WAV	-	A Digitized Sound File Format for Microsoft Windows
Windows	-	Type of Operating System Manufactured by Microsoft
WMA	-	Windows Media Audio Format Similar to MP3
WR	-	Write Pin on Integrated Circuit

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1.0 INTRODUCTION

Curtin University of Technology has a large amount of audio files stored on tapes and audiocassettes. The content of these archives is, by and large, speech. The primary purpose of this audio digitisation project is the preservation and play back of these audio contents.

The high speed audio to universal serial bus (USB) interface has been designed, to fulfil the requirements of the digitising process by sampling the line level audio and converting it into a digital format and then transmitting data over a USB connection to a host computer for storage.

The audio signal has been designed to receive a standard line level audio played at a maximum speed compression factor of 20. The audio signal will be filtered for noise reduction and sampled at a maximum sample rate of 500,000 samples per second (sps), this is to ensure that a 90 minutes of audio can be recorded in approximately four minutes to a host computer running either Windows or MAC operating system.

2.0 CONCEPT OF OPERATIONS

The high speed audio interface is based on a simple continuous stream of raw data sent from the audio interface to the host via a standard USB 2.0 full speed format. Standard line level audio signal is applied to the audio input where a series of high and low pass filters are used to reduce any background noise and distortion prior to the amplification and digitisation process.

A pre-amplifier with a small gain is used to increase the incoming audio level, prior to being digitised by the analogue to digital converter (ADC). The ADC digitises the analogue waveform into an 8-bit unsigned binary value, which is stored a in volatile 64k byte random access memory (RAM) array buffer. A programmable one MHz oscillator and logic controller are used to provide the time sequence required to interface the ADC, the buffer, and the USB module. The USB module provides a conduit for the raw binary data to be accessed from the buffer by the host machine. Figure 2-1 provides a simple block diagram of the overall audio interface process.

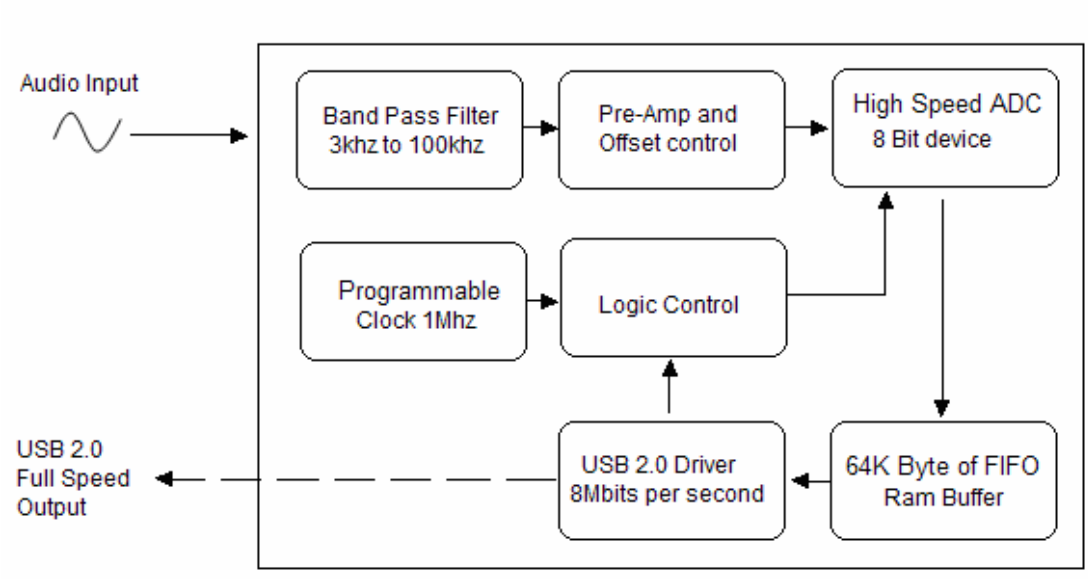


Figure 2-1: Block Diagram of Interface

3.0 THEORY OF DIGITISING AUDIO

An audio waveform is a continuously varying signal. It changes from instant to instant and as it changes between these two values it passes through all the values in between. However, this range is limited to the amplitude and frequency of the audio signal as shown in Figure 3-1.

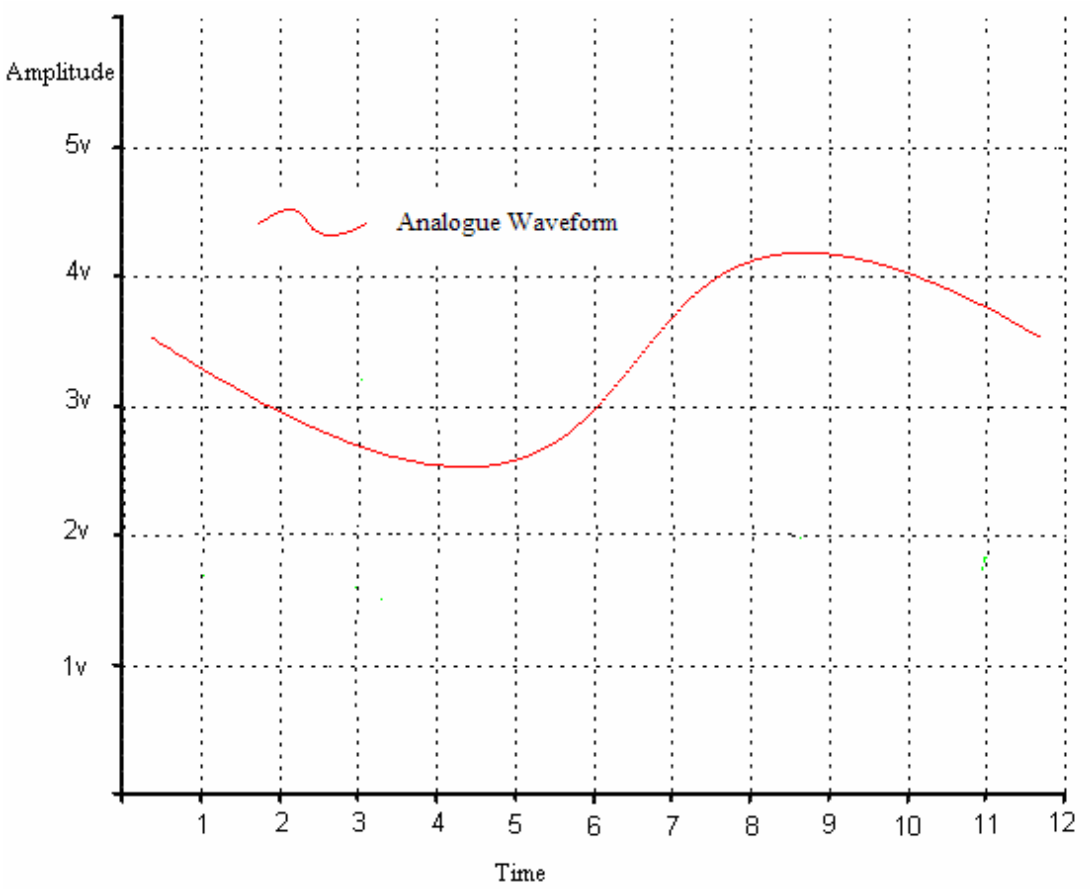


Figure 3-1: Analogue Waveform

The process of converting an infinitely changing analogue waveform into a discrete digital value, that can be recognised by a computer system, is achieved by taking discrete samples of the waveforms amplitude at regular time intervals, the higher the sample rate is the more accurate the reconstructed waveform.

3.1 Sample Rate

Sample rate defines the number of samples that are recorded per second. It is measured in Hertz or Kilohertz. Table 3-1 describes four common benchmarks for audio quality, however the audio will be played at high speed and a factor of 20 has been applied.

Samples made per second (SPS)	Description
8 KHz (160 KHz)	Standard fixed line telephone audio quality.
11 KHz (220 KHz)	At 8-bits, mono produces reasonable voice quality at a full file size.
22 KHz (440 KHz)	22k, half of the CD sampling rate. At 8-bits, mono, good for a mix of speech and music. At 16-bits, reasonable stereo quality for speech and music.
44.1 KHz (882 KHz)	A standard audio CD sampling rate.

Table 3-1: Sample Frequencies

The audio quality will improve as the number of samples per second increases. The higher the sample rate that can be achieved the more accurate the reconstruction of the original analogue waveform that can be reproduced, from the digital audio file, as shown in Figure 3-2.

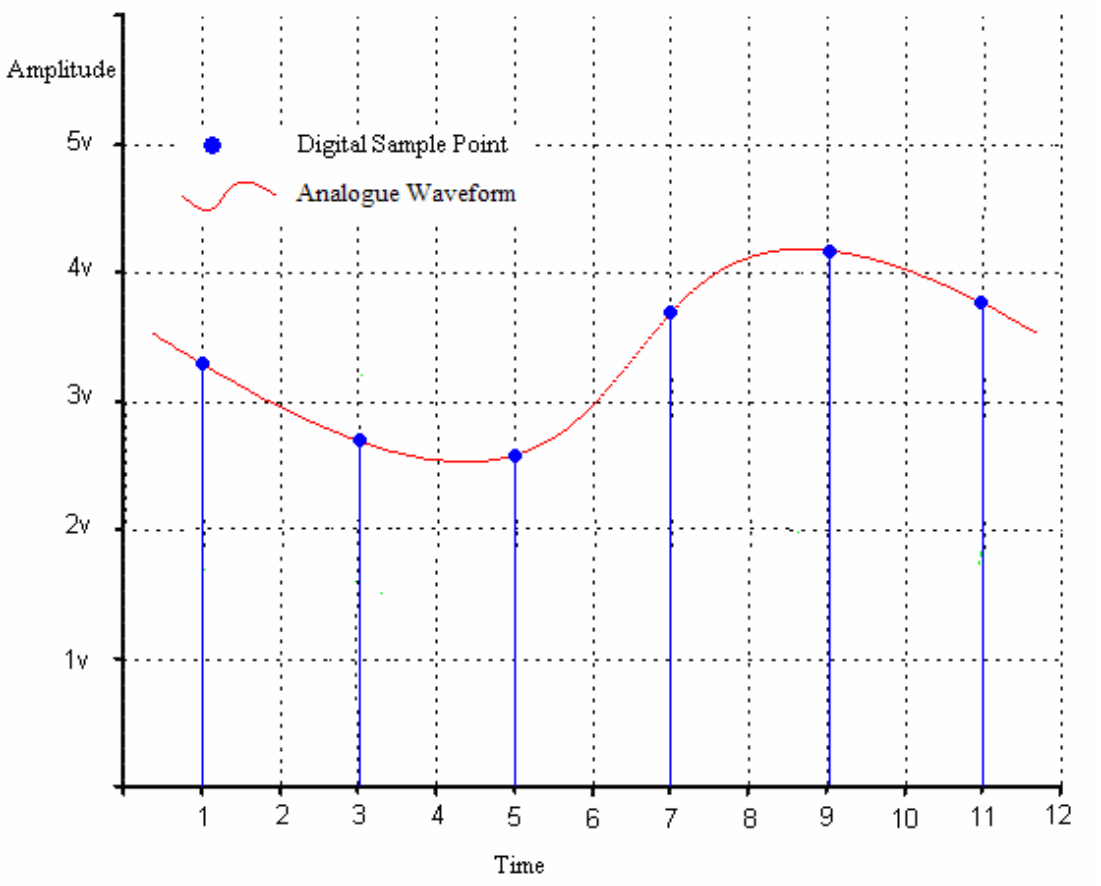


Figure 3-2: Digital Sampling

To record a high quality compact disc audio a sample rate of 882 ksps should be used. Since the audio for this project will be taken from an existing recording, a sample rate 882 ksps will produce an overly large file size for the quality of audio required therefore the audio interface is limited to a maximum sample rate of 500 ksps.

3.2 Bit Rate

The bit rate indicates the amount of audio data that is being transferred at any given time. The bit rate can be recorded in two ways, variable or constant. A variable bit rate creates smaller files by removing inaudible sounds. Therefore, it is suited for applications where bandwidth is a consideration.

A constant bit rate, in comparison, records audio data at a set rate irrespective of the content. This produces a replica of an analogue recording, even reproducing potentially unnecessary sounds. As a result, file size is significantly larger than those encoded with variable bit rates. Table 3-2 indicates how a constant bit rate affects the quality and file size of an audio file.

BIT RATE	QUALITY	MB/MIN
1411	CD audio	10.584
192	Near CD quality	1.440
128	Typical music level	0.960
112	Digital radio quality	0.840
64	FM quality	0.480
32	AM quality	0.240
16	Short-wave quality	0.120
8	Audio quality	0.06

Table 3-2: Bit Rates

3.3 Nyquist Theory

Discrete time sampling is a process where a signal is measured periodically at evenly spaced intervals. An input analogue signal ($x_a(t)$) is to be sampled continuously at all points in time. Therefore, if $x_a(t)$ is multiplied by the analogue signal waveform ($p(t)$), where $p(t)$ is a series of evenly spaced delta functions that occur every Ts seconds, then the sampling frequency (f_s) will be.

$$\text{Sample Frequency (fs)} = \frac{1}{Ts} \qquad (3.1)$$

Each delta function will take a sample (n) based on its location in time and therefore the sample point in time.

$$\text{Sample point in time (t)} = n \bullet Ts \tag{3.2}$$

The value of t may be used to represent the location of each sample point in time of the analogue signal therefore can be represented by x[n].

$$X[n] = \sum_{m=\infty}^{\infty} [Xa(n \bullet Ts) \bullet \delta(n \bullet Ts - m \bullet ts)] \tag{3.3}$$

The frequency domain, of $x_a(t) * p(t)$ looks like the frequency domain of $x_a(t)$ shifted either up and down by the integer value, which are multiples of f_s. If f_s is at least twice the maximum frequency of $x_a(t)$, the frequency spectra of $x_a(t) * p(t)$ will not overlap. Therefore, if $x_a(t) * p(t)$ is a low pass filtered the original $x_a(t)$ signal can be recovered perfectly.

This is the most important rule of sampling proved by Shannon and Nyquist. It proves that band limited signal can be perfectly recreated from its discrete time samples so long as the sampling frequency is at least twice as high as the maximum frequency of the original band limited signal. The maximum frequency that can be sampled by a given sampling system is called the Nyquist frequency.

If samples are taken at less than twice the original frequency (Nyquist frequency) a problem starts to occur, called aliasing. This is where a much lower frequency is reconstructed from the limited amount of sample points obtained from the original high frequency, as shown in Figure 3-3.

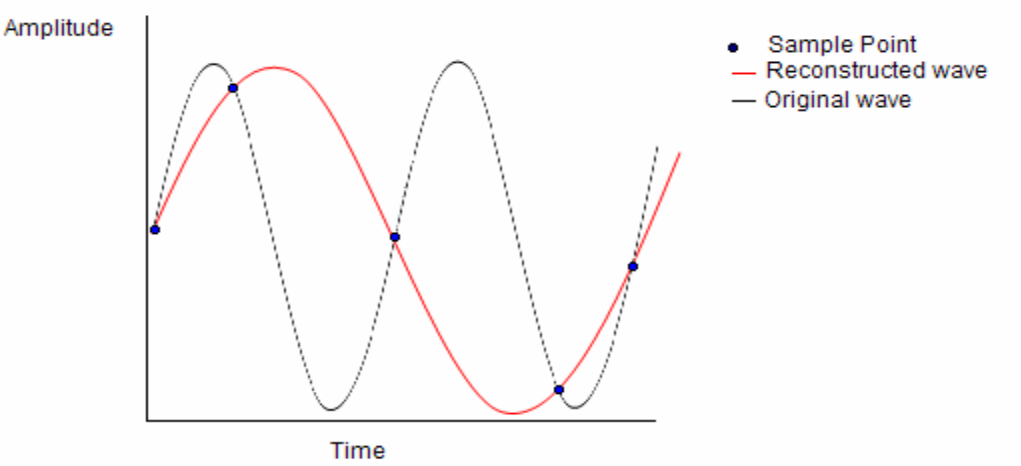


Figure 3-3: Aliasing Sample Frequency

3.4 Digital Audio Formats

The majority of audio formats use lossy compression to reduce the file size by removing superfluous audio data. Master audio files should ideally be stored in a lossless format to preserve all audio data, as shown in Table 3-3. The audio interface has been designed to deliver a high rate of raw unsigned 8-bit data via a USB port.

FORMAT	COMPRESSION	STREAMING SUPPORT	BIT-RATE	POPULARITY
MPEG Audio Layer III (MP3)	Lossy	Yes	Variable	Common on all platforms
Mp3PRO (MP3)	Lossy	Yes	Variable	Limited support
Ogg Vorbis (OGG)	Lossy	Yes	Variable	Limited support
RealAudio (RA)	Lossy	Yes	Variable	Popular for streaming
Microsoft Wave (WAV)	Lossless	No	Constant	Primarily for MS Windows
Raw Binary Data ASCII	Lossy	Yes	Constant	Limited support
Windows Media (WMA)	Lossy	Yes	Variable	Primarily for MS Windows

Table 3-3: Audio Formats

4.0 AUDIO INTERFACE COMPONENTS

The following section provides an in detail description of the individual components that are used in the design of the audio interface.

4.1 Power Supply

There are many types of power supplies, most are designed to convert high voltage AC mains electricity to a suitable low voltage supply, for electronics circuits and other devices. For an ideal voltage regulator, the output voltage would be pure direct current (DC) however in a real supply there will always be noise at the output stage of the regulator.

The use of clean regulated voltages in audio circuits is important, as operational amplifiers use a DC supply voltage. If the power supply output is a perfect DC, the operational amplifier output would be based solely on its input. If noise is allowed to be introduced into the power supply the noise will be amplified by the operational amplifier and treated as part of the analogue signal that is being digitising.

The Texas Instrument, PT5101 integrated switching regulator (ISR), produces a very clean five volts DC line regulation, to within 1.5% of the specified output voltage with less than a 2% ripple. The PT5101 provides an excellent performance in both noise reduction and heat dissipation in the T0220 style package this noise reduction and heat dissipation makes it an ideal choice for low powered audio applications, such as this audio interface. The performance characteristics of PT5101 regulator is detailed in Table 4-1.

CHARACTERISTIC	CONDITIONS	MIN		TYPE	MAX	UNITS
Output Current	Over Vin Range	0.1		—	1.0	A
Input Voltage Range	Over Io Range	9	—	—	38	VDC
Set Point Voltage Tolerance		—	—	±1	±2	%Vo
Temperature Variation	0° ≤Ta ≤ +60°C, Io=Iomin	—	—	±0.5	—	%Vo
Line Regulation	Over Vin Range	—	—	±5	±10	mV
Load Regulation	Over Io Range	—	—	±5	±10	mV
Total Output Voltage Variation	Includes set-point, line, load, 0° ≤Ta ≤ +60°C	—	—	±1.5	±3	%Vo
Efficiency		Vo=5.0V	—	90	—	%
Vo Ripple (pk-pk)	20 MHz Bandwidth		—	2	—	%Vo
Switching Frequency	Over Vin range	Vo ≥ 5.0V	500 575	650 725	800 875	K Hz
External Output Capacitance			100	—	—	µF
Operating Temperature Range	Over Vin Range		–40	—	+85	°C

Table 4-1: PT5101 Characteristic

4.2 High and Low Pass Filter Requirements

The first device required in the ADC process is an analogue low and high pass filter, whose sole function is to band limit the input signal without introducing excessive linear or nonlinear distortion and without generating excessive noise. Any introduced noise generated at this stage will be treated as part of THE genuine audio signal and will be digitised.

The audio interface has been designed based on normal voice audio characteristics, which have a frequency range of 150 Hz through to 5000 Hz. A compression factor of 20 is being used; this now has the effect of extending the audio signal from 3000 Hz through to 100 KHz, as shown in Figure 4-1.

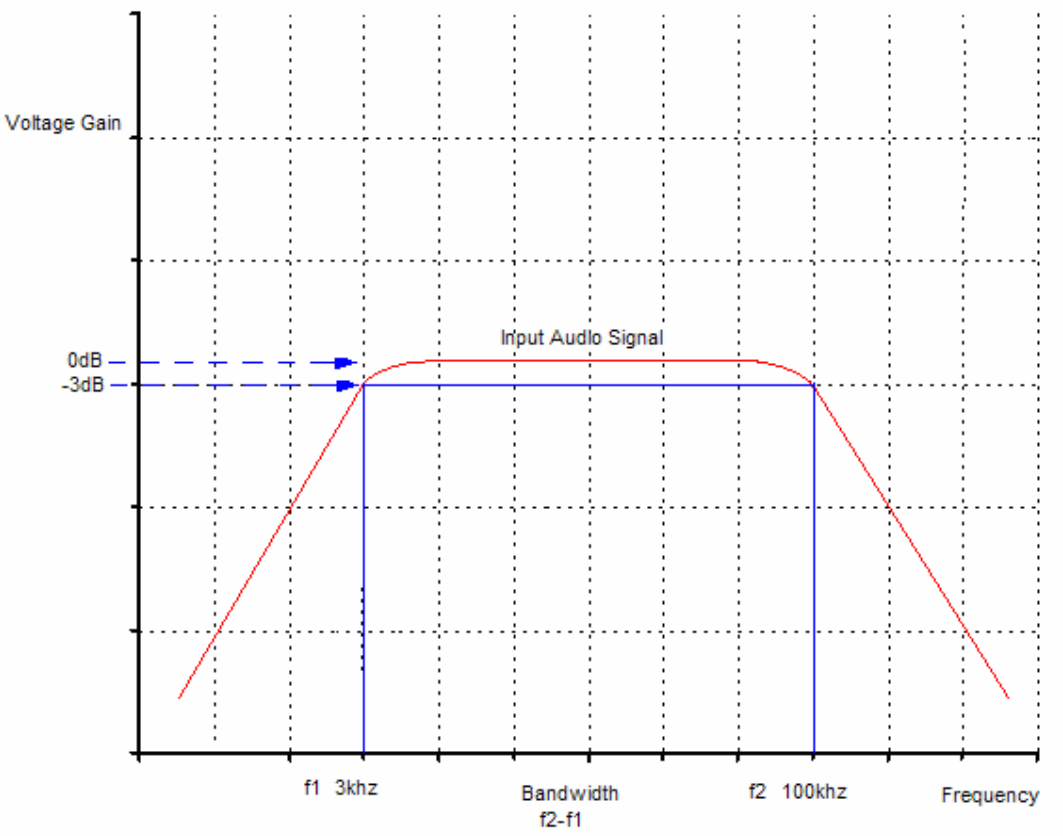


Figure 4-1: Bandwidth

4.3 High Pass Filter

The high pass filter passes all the frequency bands above a certain point and eliminates all the frequencies below that point. The point at which this transition occurs is called the corner frequency. The effectiveness of the high pass filter can be assessed on how steep the gain drops away from the corner frequency.

The high pass filter design is based around the Texas Instrument dual TLV2772 operational amplifier. This integrated circuit (IC) has been configured to operate from a single five volt supply rail with a unity gain.

Like any electronic device the operational amplifier needs to be correctly biased if it is to function properly. The most appropriate DC biasing in this case is 50% of the supply rail. Two resistors R1 and R2 are used to provide the operational amplifier with this biasing, as shown in Figure 4-2.

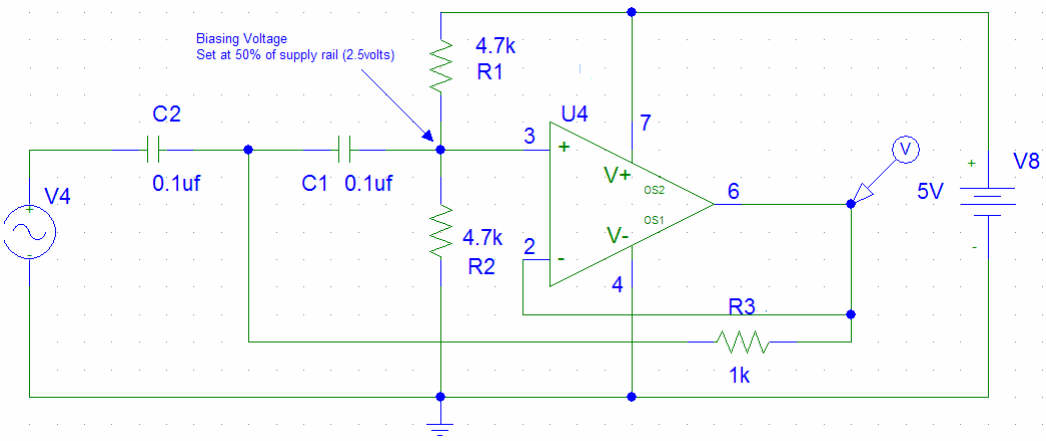


Figure 4-2: High Pass Filter Schematic

The biasing point is used as an offset for the incoming analogue signal, this is to ensure that both the positive and negative parts of the signal are presented to the input of the amplifier without the risk of clipping, as shown in Figure 4-3.

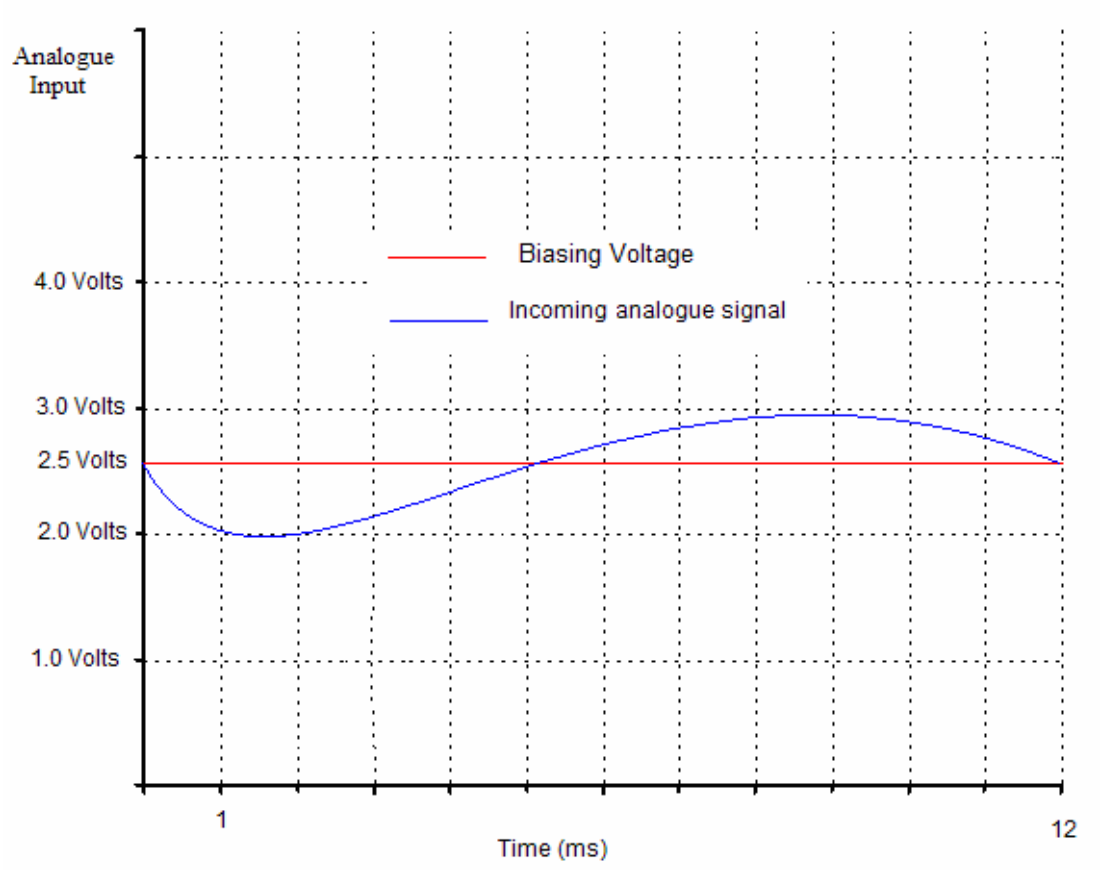


Figure 4-3: Amplifier Offset Biasing

The second order high pass filter for the audio interface has been designed to start eliminating unwanted frequencies below 3000 Hz. The standard for measuring this corner frequency is minus three decibel or 50% below the original output. For a second order filter, the corner frequency can be calculated using the following formula 4.4, the result are shown in Figure 4-4.

$$\text{Corner Frequency} = 1 / (2 * \pi (R3 * R2 * C1 * C2)^{0.5} \quad (4.1)$$

Corner Frequency = 732 Hz

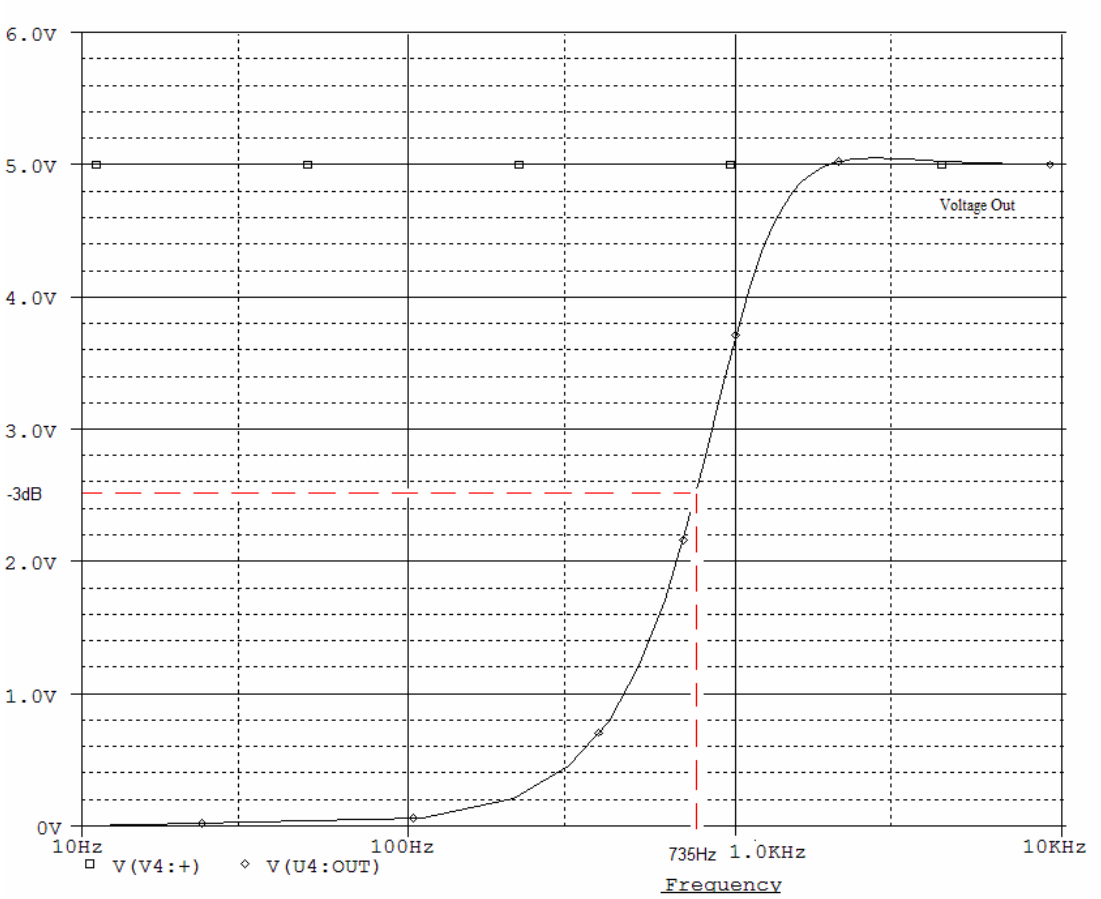


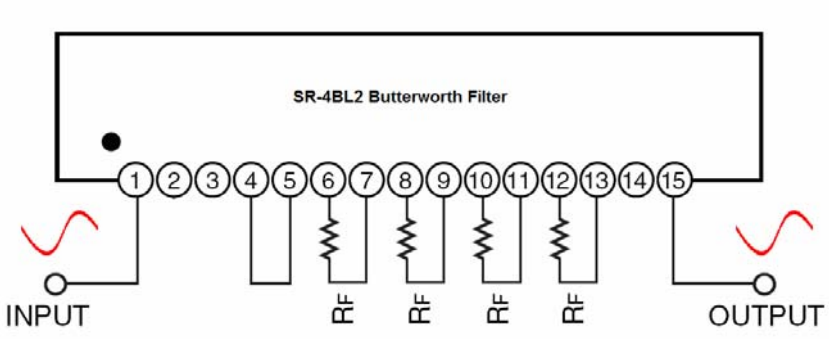
Figure 4-4: High Pass Filter Frequency Response

4.4 Low Pass Filter

Similar to the high pass filter, a low pass filter is designed to pass all frequency bands below a certain point and eliminate all the frequencies above that point. The point at which this transition occurs is called the corner frequency. The effectiveness of the low pass filter can be assed by how steep the gain drops away above the corner frequency.

The low pass filter used for the audio interface is an SV-4BL2 Butterworth filter. The filter is pre-manufactured into a 15-pin single in line package supplied by NF Corporation. The SV-4BL2 filter operates from a single five volt supply rail and will require no biasing,

The SV-4BL2 Butterworth filter can be tuned to start eliminating frequencies, anywhere in the range from 100Hz through to 100 KHz. This is achieved by selecting the four external resistors (RF) to calculate the corner frequency as shown in Figure 4-5.



RF = 1.6K minimum and 1.6M maximum

Figure 4-5: SR-4BL2 Tuneable Butterworth Filter

The SV-4BL Butterworth filter was selected for its rapid drop off in gain for all frequencies above the 100 KHz frequency corner point. Figure 4-6, shows that the filter will provide a reduction in the output signal of -24 dB for all frequencies above 200 KHz, therefore if a five volt sinusoidal waveform is applied to the input the output signal will be reduced to less the 19.53mV.

The ADC is unable to detect any changes in the input voltage, of less than 19.53mV. Therefore, if the ADC is unable to detect any changes in the input stage then no change in the digitised output stage will occur. This will have the effect of eliminating all discrete digital values for frequencies above the 200 KHz point, as shown in Figure 4-6.

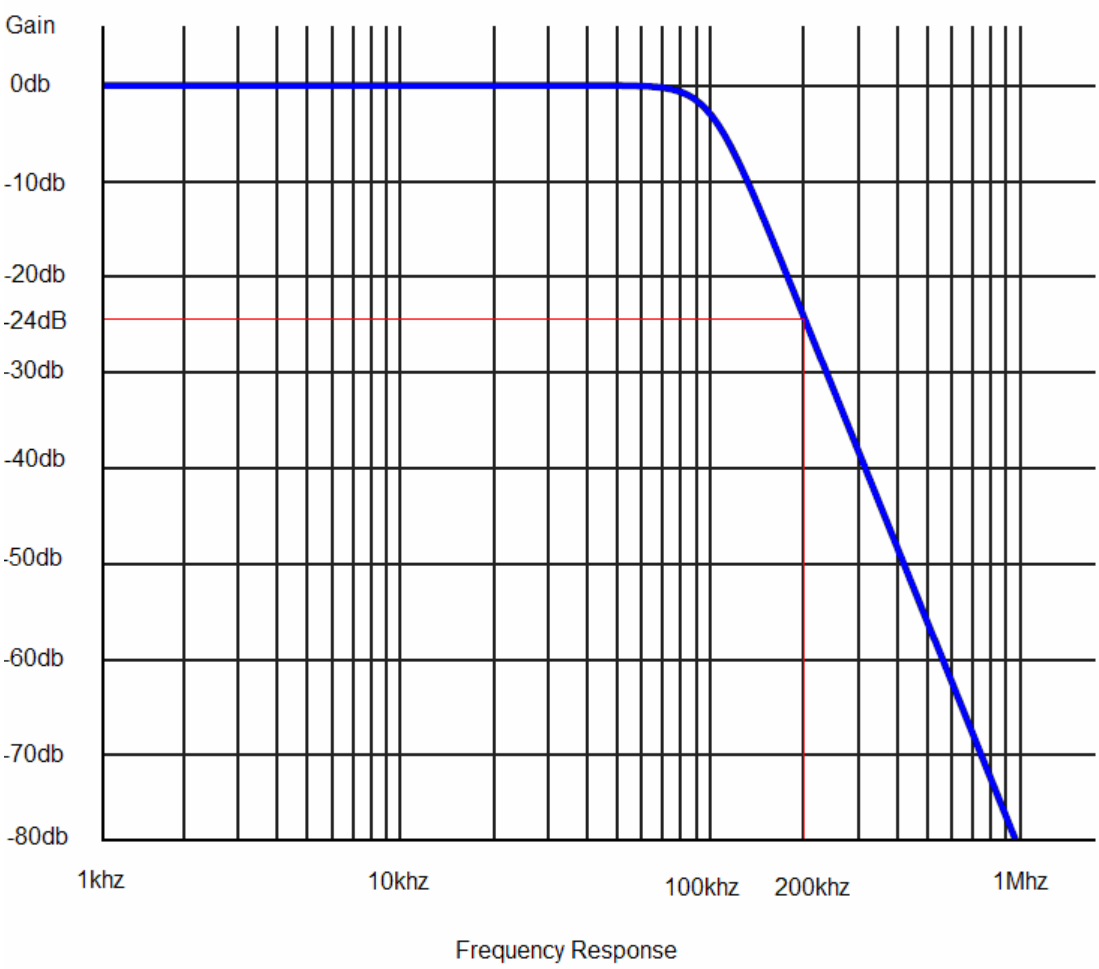


Figure 4-6: dB Frequency Response

4.5 Amplifier and Offset Control

An audio waveform is a continuously varying signal. It changes from instant to instant, and as it changes between the two values it passes through all the values in between, as shown in Figure 4-7.

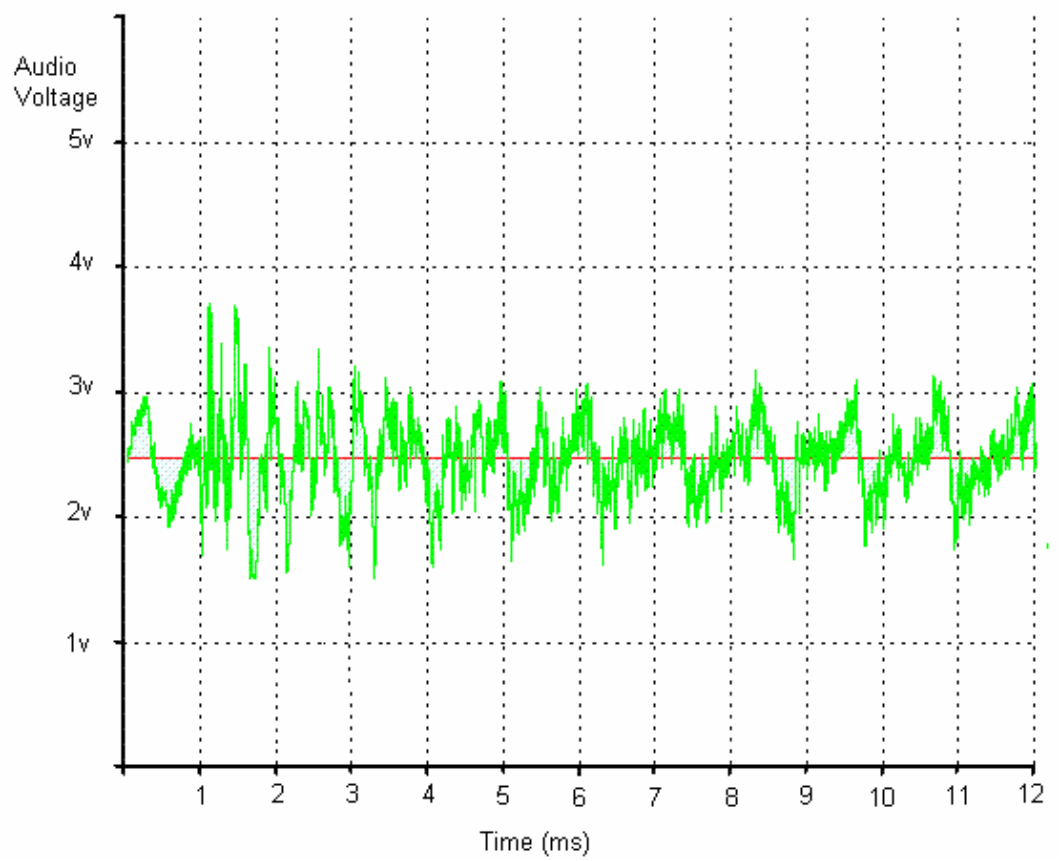


Figure 4-7: Audio Voice Waveform

The audio interface has been designed to accept a standard audio line level signal which has a maximum of two volts peak to peak. The audio interface is able to digitise an analogue waveform with a maximum of five volts peak to peak. Therefore, to take advantage of the full scale resolution of the device a small pre-amplifier has been added to increase the audio waveform. The pre-amplifier is based around the Texas Instruments TLV2772 operation amplifier, and has been configured to produce an overall gain in the range 1.1dB to 11dB. Figure 4-8 show the schematic circuit diagram of the pre-amplifier.

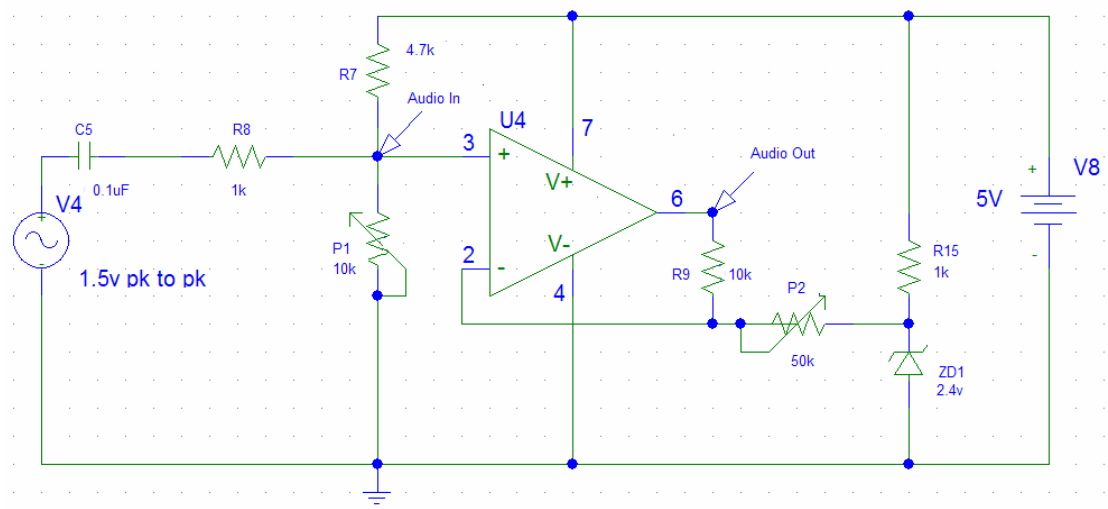


Figure 4-8: Pre-amp and Offset Schematic

The operation amplifier is able to achieve this variable gain control by providing feed back through a voltage divider resistor network R9 and P2, as shown in Figure 4-8. The amount of gain the operation amplifier has is proportional to the ratio of resistance between R9 and P2.

$$\text{Amplifier Gain} = ((R9 + P2) / P2) \qquad (4.2)$$

Figure 4-9 shows a comparison between the input waveform and the output waveform of a preamplifier with an overall gain of 1.6 dB set.

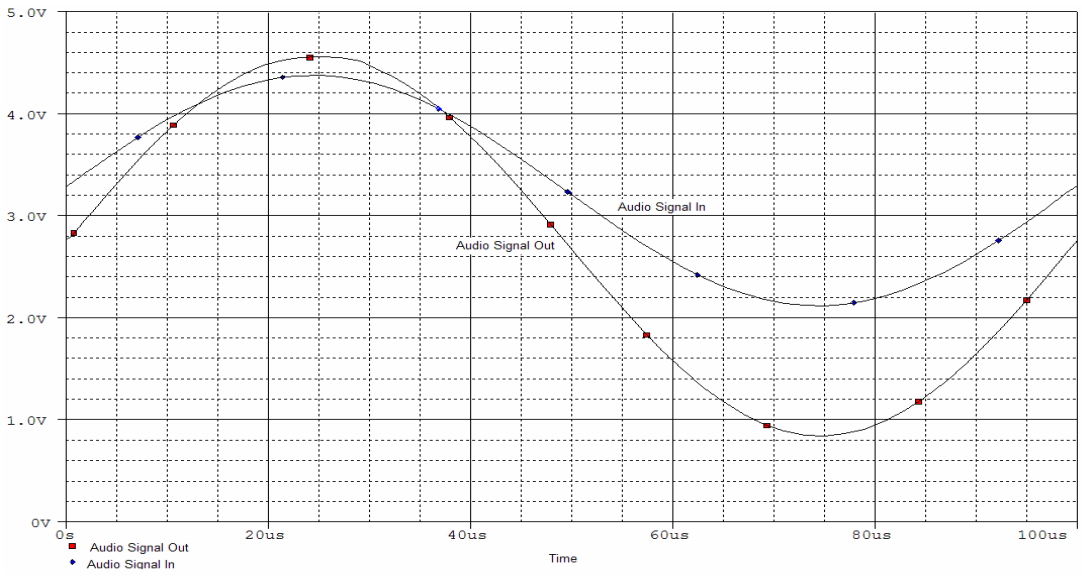


Figure 4-9: Pre-amp Output Waveform

4.6 Timing Clock

A dipswitch selectable programmable crystal oscillator provides timing for both the ADC and USB interface module.

The USB interface read sequence is clocked at the fixed fastest rate of 1 MHz, whilst the ADC is clocked at a maximum rate of 500 KHz. This difference in clocking speed is to ensure that the ADC does not produce data quicker than the USB interface is able to transfer the data to the host.

A six channel dipswitch enables the user to manually select a total of 62 different sample rates, as detailed in Table 4-2. This gives the advantage of being able to limit the size of the files produced over a fixed period of sampling time. However, by sampling the analogue waveform at the slower rate will result in a loss of quality and accuracy of the original analogue signal.

Switch		Switch 6		0	0	0	0	1	1	1	1
		Switch 5		0	0	1	1	0	0	1	1
Switch 3	Switch 2	Switch 1	Switch 4	0	1	0	1	0	1	0	1
0	0	0		N/A	100K	10K	1K	100	10	1	1/10
0	0	1		100K	10K	1K	100	10	1	1/10	1/100
0	1	0		500K	50K	5K	500	50	5	1/2	1/20
0	1	1		333.3K	33.3K	3.3K	333.3	33.3	3.33	1/3	1/30
1	0	0		250K	25K	2.5K	250	25	2.5	1/4	1/40
1	0	1		200K	20K	2K	200	20	2	1/5	1/50
1	1	0		166.6K	16.6K	1.6K	166.6	16.6	1.6	1/6	1/60
1	1	1		83.3K	8.3K	833.3	83.3	8.3	0.83	1/12	1/120

Table 4-2: Dipswitch Frequency Selection

4.7 Analogue to Digital Converter

The AD7820 ADC is an 8-bit, 1Msps (conversion time of 660ns) linear compatible CMOS (LC^2MOS) device providing 100 KHz of bandwidth, by utilising half flash conversion technique. This technique not only eliminates the need for an external clock signal, but also performs ADC at a very fast rate whilst drawing a minimal current.

The operating principle of the parallel flash ADC is based on a large number of comparators, which compares the input voltage to a set of reference voltages across a resistor network, as shown in Figure 4-10.

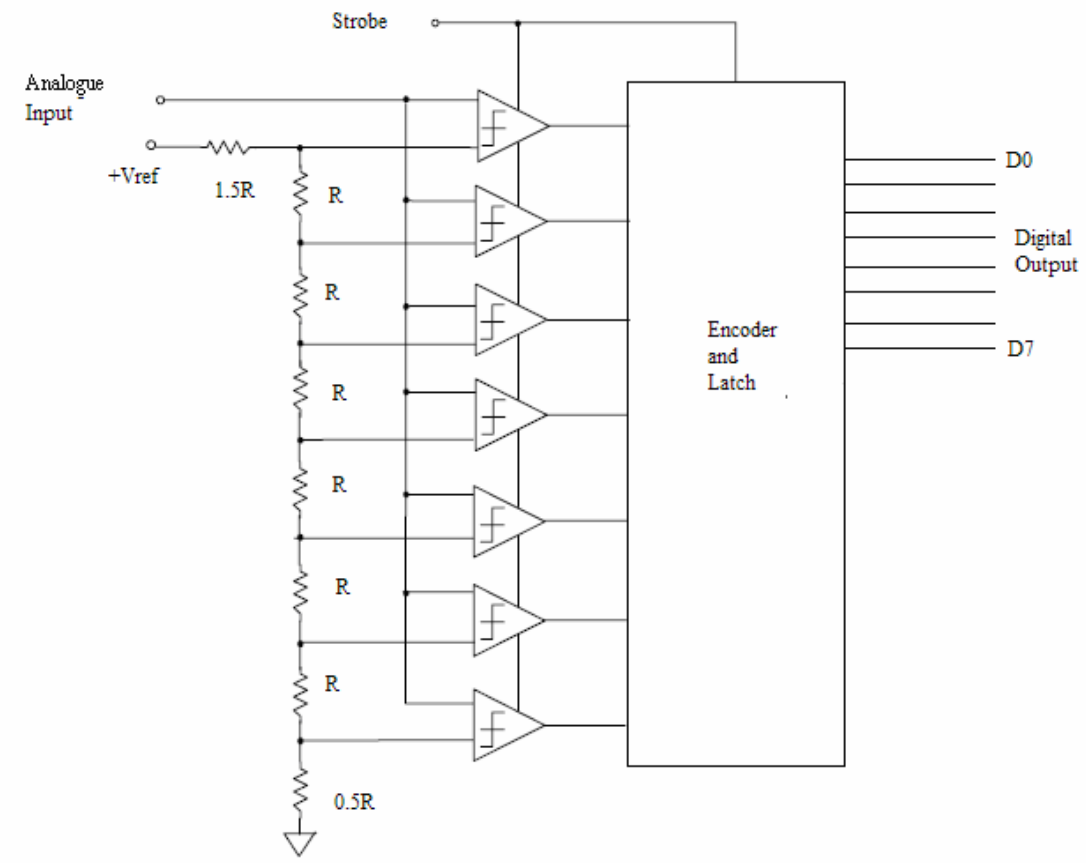


Figure 4-10: ADC Full Flash

This arrangement will produce a very fast conversion time, which is equal to one comparators propagation delay, as all comparators are checked simultaneously. An ADC of this type will require 2^N-1 (N is the number of bits) comparators. For an 8-bit device a total of 255 comparators would be required. This large quantity will not only takes up valuable space on the silicone die, but will also draw a large amount of current. To resolve this issue a half-flash ADC was used. The half flash ADC performs the same as the flash ADC but uses far less comparators. For a 8-bit device only 30 comparators are used, this is achieved by combining the results of two 4-bit flashes to produce a single 8-bit valve. A block diagram of the half flash ADC device is shown in Figure 4-11.

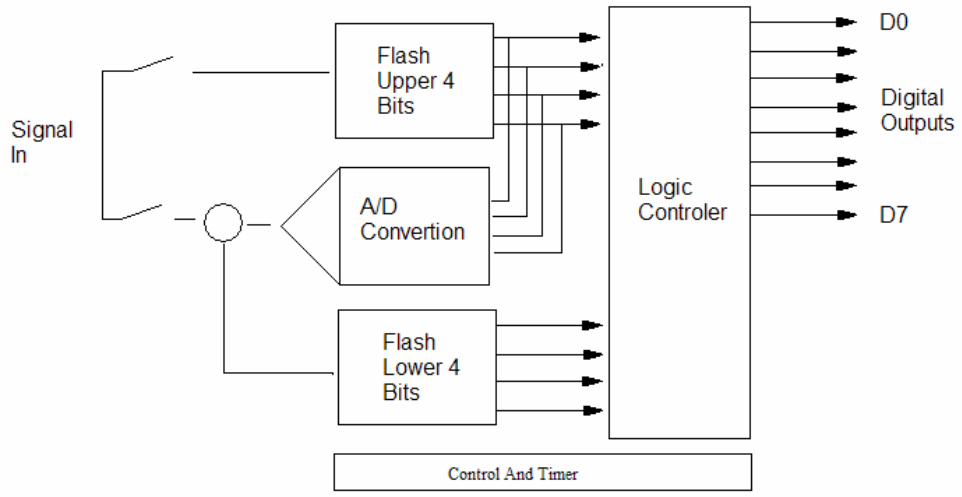


Figure 4-11: ADC Half Flash

After the conversion has been completed, a binary value that represents the analogue voltage being sampled is available across the data bus D0 to D7. Figure 4-12 shows a comparison between the analogue and digital values.

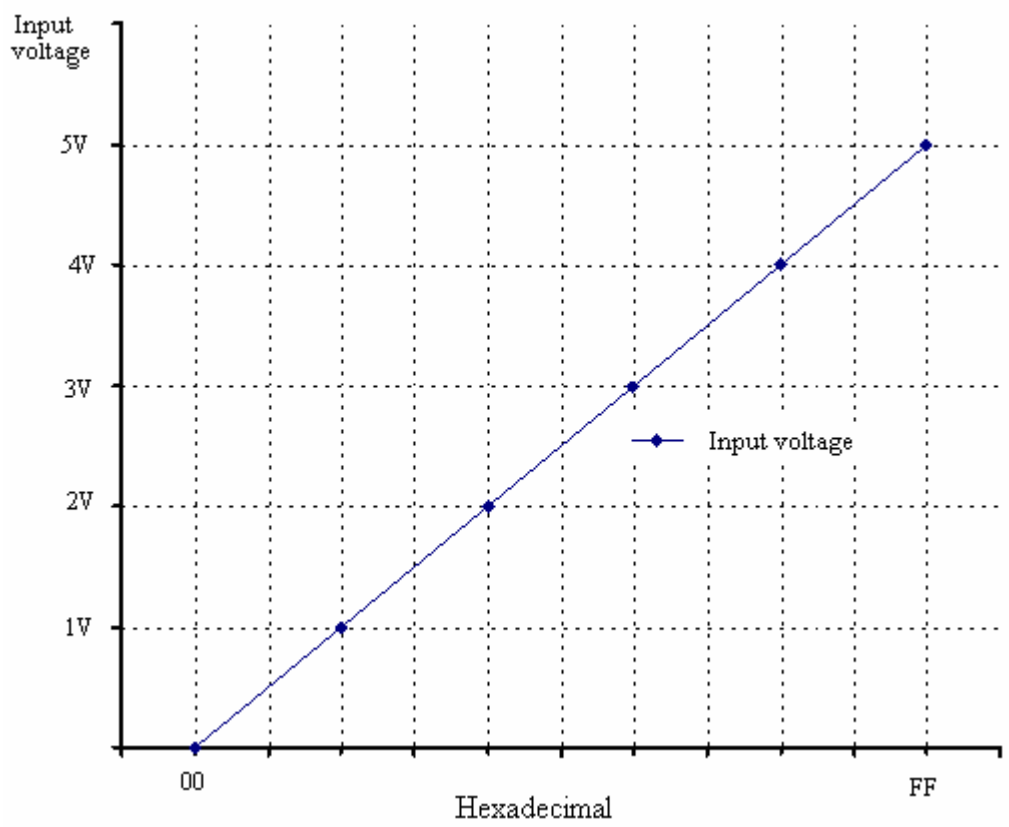


Figure 4-12: Analogue to Hexadecimal Conversion

4.8 Quantisation Errors

Discrete time sampling is the first step to digitisation of audio. However, the zero loss properties of discrete time sampling depends on the ability to perfectly measure the exact value of each sample and reproduce it in both time and amplitude. Quantisation is the process of converting the analogue signal to a digital value, the number of discrete values available will depend on the number of bits being used. The AD7820 ADC uses a total of 8-bits, this gives a total of 256 possible discrete values (2^8). One discrete value is therefore equal to the reference voltage divided by 2^8, as shown in Figure 4-13.

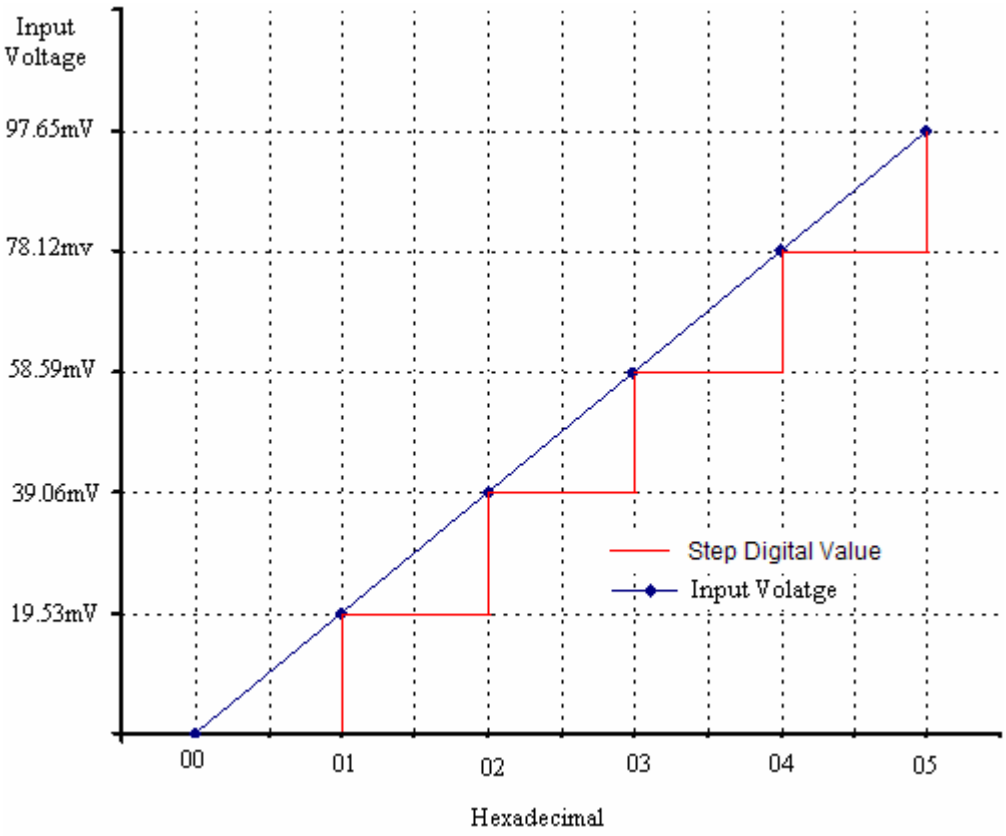


Figure 4-13: Quantisation Error

$$\text{One discrete value} = \text{five volts} / 256 \qquad (4.3)$$

$$\text{One discrete value} = 19.53\text{mV}$$

Normally, the quantised levels are spread linearly throughout the peak to peak range of the converter, as shown in Figure 4-13, because of this linearity no single sample can have an error greater than half of one quantisation level. The error between the original signal and the quantised level can cause a loss in quality in the digitised values of the original waveform.

4.9 Logic Control Gates

The logic used to control the high speed audio interface is made up of two different logic gates, the 74LS04 hex inverter and the 74LS132 Schmitt triggered NAND gate.

The logic gates are used to provide the logic control and time critical switching between the timing clock, ADC, memory buffer and USB module. The ADC is clocked at regular sampling rate intervals. The sampling rate frequency is determined by the frequency selected by the six channel dipswitch.

The conversion process starts on the falling edge of every clock signal, the clock signal drives the ADC chip select (CS) and read (RD) pins low. Once the conversion process has started, 50ns later the ready control line (RDY) pin is driven low, after a further 666ns, when the conversion process is completed, the ready control line is driven high. This transition from low to high is used to latch the valid data into the memory buffer. The ADC will place valid data on the data bus 30ns after the ready line is driven high, as shown in Figure 4-14. However, due to the propagation delay and the internal capacitance of the ADC this transition on the ready line will not be received by the memory buffer for at lest another 40ns. The 40ns delay will allow sufficient time for the ADC to place and stabilise the valid data on the data bus.

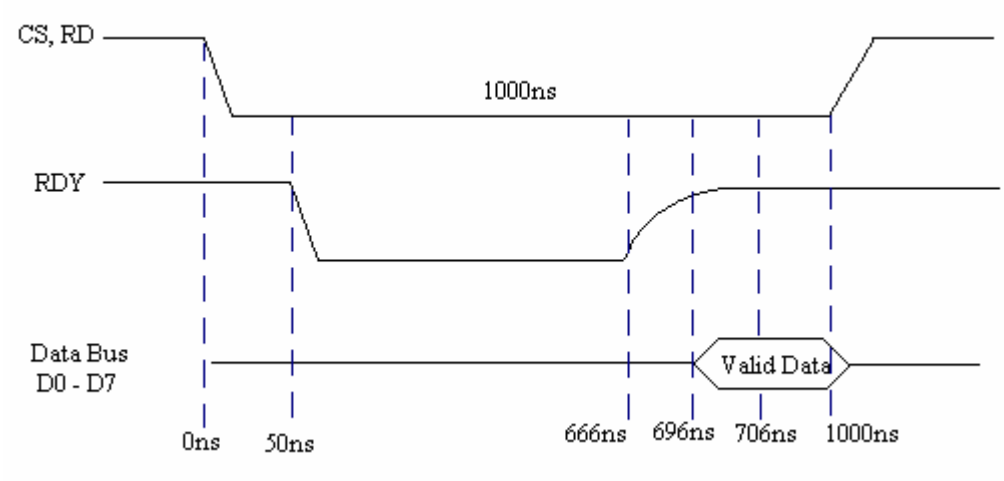


Figure 4-14: Buffer Write Sequence

4.9.1 Memory Write Operation

The audio interface memory buffer is configured in a first in first out (FIFO) memory array. When the buffer contains at least one byte of data, the empty flag (EF) control line transitions from a low to a high. This transition enables the 1 MHz clock timing signal to be gated though the logic gate sequence, as shown in Figure 4-15 and the logic truth table in Table 4-3.

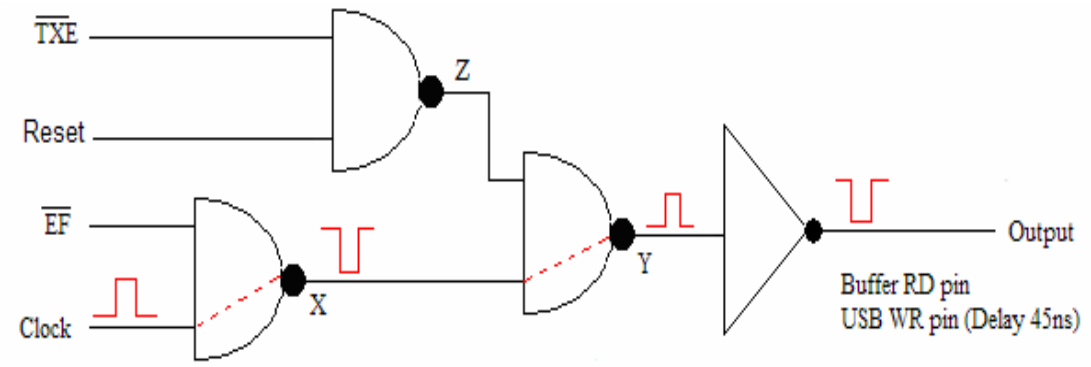


Figure 4-15: Buffer Read USB Write Logic

/TXE	/EF	CLOCK	X	Y	Z	OUTPUT
0	0	0	1	0	1	1
0	0	1	1	0	1	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	1	1	0	0
1	0	1	1	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0

Table 4-3: Buffer Read and USB Write Truth Table

4.9.2 Memory Read Operation

Data is read from the memory buffer by applying a transition from a high to a low on the read line (RD) of the memory buffer. After 10ns this read line becomes low and valid data will be available on the data bus D0-D7. This same transition used to read the data from the memory buffer is also used to latch the data into the USB module. However, to ensure the memory buffer has placed and stabilised the valid data on the data bus D0-D7, the transition has been delayed by 45ns. The USB module also provides feedback to the logic gate by driving the transmit line (TXE) high. This is to ensure that no data can be written to the USB module whilst the host is retrieving data. Figure 4-16 shows the sequence of a memory read and USB write operation.

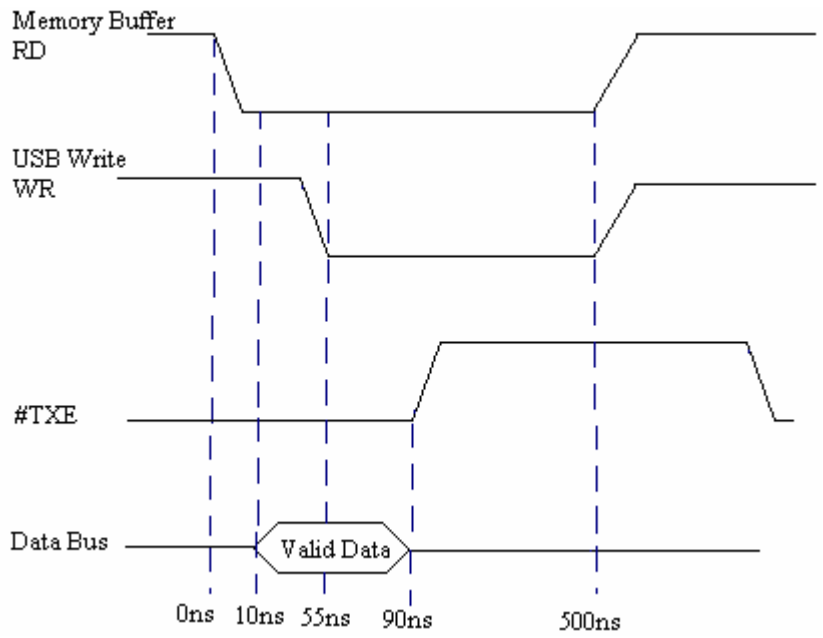


Figure 4-16: Memory Read and USB Write Operation

4.10 First In First Out Memory Buffer

A CY7C466 is a volatile 64K byte random access memory (RAM) buffer where the memory is organised, such as data is read out of the buffer in the same order as the data was written; this type of memory is commonly known as first in FIFO.

This memory device provides a temporary storage of the digitised analogue waveform obtained from the ADC; this buffering is to ensure that no loss of data occurs whilst the USB interface module is being serviced by the host during data transfer. This type of memory is ideal for this application, as the ADC will be accessing the memory at a much slower rate but at regular intervals. However, the USB module will be accessing the data at a much faster rate, but at irregular intervals.

Due to the speed at which the ADC will be writing data to the memory buffer, a 64k byte memory will provide a maximum buffering of 128ms of audio stream sampled at a maximum of 500k sps. If a slower rate of sampling is selected, on the six-channel dipswitch, then the amount of audio stream stored by the buffer can be increased. Table 4-4 shows the comparison between the sample rate and the audio stream stored within the memory buffer.

Sample Rate (Ksps)	Audio held in memory played at standard rate (seconds)	Audio held in memory played at factor 20 (seconds)
500	0.128	2.560
333	0.192	3.844
250	0.256	5.120
200	0.320	6.400
166	0.386	7.711
100	0.640	12.800
83	0.771	15.422
50	1.280	25.600
33	1.939	38.788
25	2.560	51.200
20	3.200	64.000
16.6	3.840	76.803
10	6.400	128.000
8.3	7.680	153.606
5	12.800	256.000
3.3	19.202	384.038
2.5	25.600	512.000
2	32.000	640.000
1.6	40.000	800.000
1	64.000	1280.000

Table 4-4: Audio Buffer

The USB module will provide a maximum transfer of 8Mbits per second, this is twice the rate at which the ADC can sample, process and deliver data to the memory buffer. By transferring data to the host at the highest rate will ensure, that even with

the USB overheads added to the encapsulated data package, that there is no loss in audio data due to the memory buffer becoming full or over running.

Data is written to the FIFO memory on the falling edge of the write control line. This falling edge starts the write sequence and the write pointer is incremented down the dual port RAM array by one to the next valuable memory location, as shown in Figure 4-17.

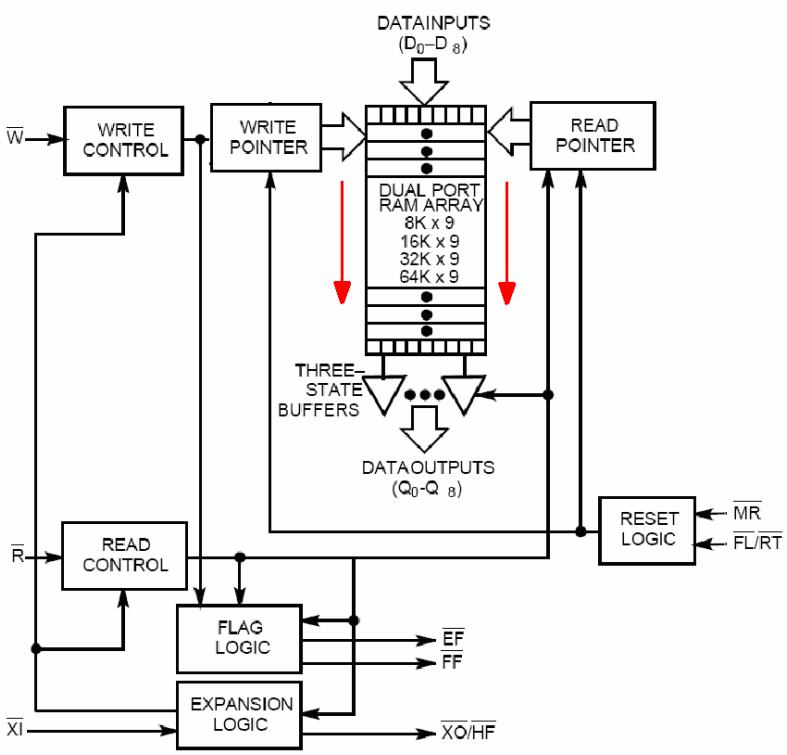


Figure 4-17: Block Diagram FIFO Memory Buffer

The 8-bit binary valve presented to the data bus pins D0 through to D8 is latched into the FIFO on the rising edge of the write control line. Once the write sequence has been completed the valid data is stored with that memory location.

When the memory device contains valid data the read pointer and write point, shown in Figure 4-17, will not point to the same location and will therefore activate the empty flag (/EF) control line. This empty flag is used to signal the external logic that data is now available to be read.

The read sequence, is initiated by the falling edge of the read control line, will only become active if the /EF is active (data in memory), if the /EF is not active the read sequence is ignored. The read pointer will increment down the dual port RAM array by one, and any data contained within that memory location will be presented on the output pins Q0 through to Q8. This process will continue until the read pointer is pointing to the same memory location as the write pointer and when this occurs the /EF control line returns to normal indicating that there is no more data to be read.

4.11 Reset and Initialisation

During power up and USB driver initialisation, the audio interface is held in a reset condition, to ensure that the internal logic and memory buffer are all reset to a known status. During power up, the audio interface is held in a reset condition and the timing clock is suspended. The timing clock will remain suspended until the host has initialised the USB module. After this initialisation process is complete the reset line is released the timing clock is started and the memory buffer is cleared by placing the read and write pointers to the same memory location at the top of the memory array stack.

4.12 USB Parallel Interface

The USB interface module is based around the FT245BM integrated circuit (IC) supplied from Future Technology Devices International (FDTI) and has been specifically designed to interface an 8-bit parallel bus structure. The processing of the USB stack, the USB transceiver and the signal conditioning is carried out by the FT245BM.

4.12.1 USB Interface Connections

The FT245BM makes use of the industry standard four-wire USB cabling system that provides +Data and -Data lines along with a five volt line and a ground line. The USB ports interfaces to the host via a type B connector with four pins, two pins on one side of the plastic pin and two pins are on the other side as shown in Figure 4-18. Table 4-5 defines the pin functionality, of the B type connector, used for this audio interface. Since the audio interface is externally powered by the PT5101 switch regulator pins one and four are unused.

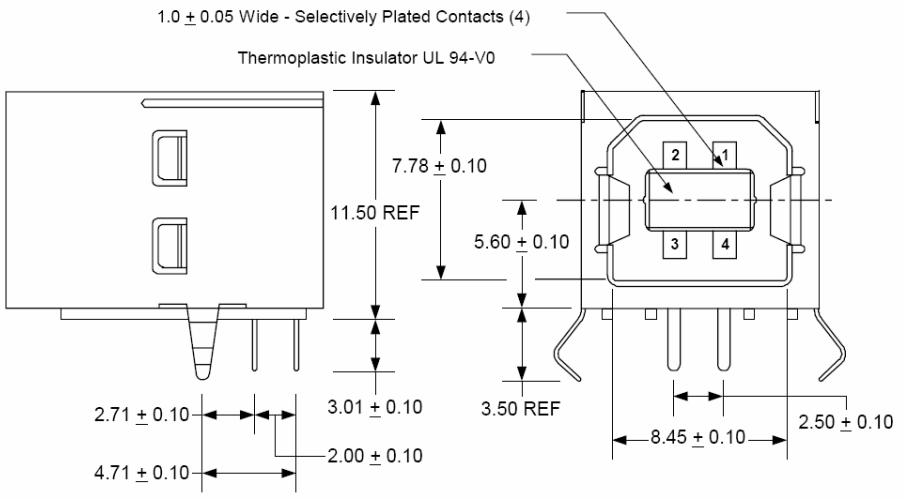


Figure 4-18: B Type USB Connector

PIN NUMBER	CABLE CORE COLOUR	FUNCTION
1	Red	+5v Supply
2	White	Data D-
3	Green	Data D+
4	Black	Ground

Table 4-5: USB Pin Identification

4.12.2 USB Data Transfer Rate

The data can be transferred at speeds that can go as high as 8Mbits per second for this audio interface, even though USB standards allow for data transfers at speeds as high as at 12Mbits.

4.12.3 USB Electrical Interface

The USB electrical interface is a differential where +Data swings between zero volts and five volts while -Data swings between five volts and zero volts at the same time, as shown in Figure 4-19.

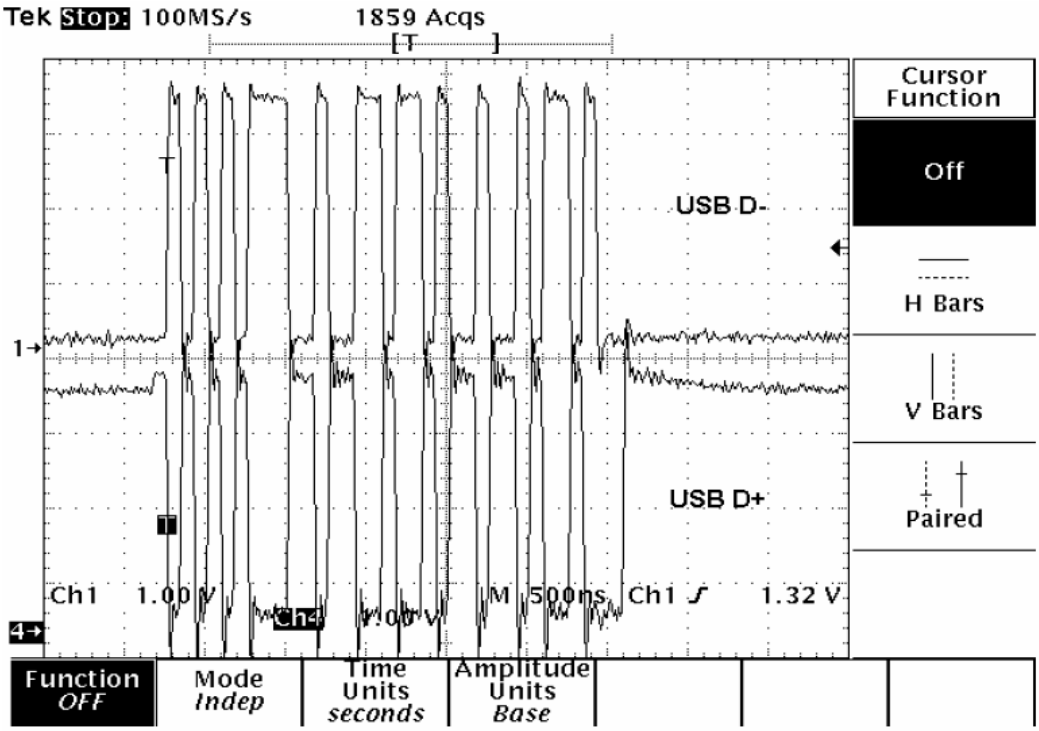


Figure 4-19: Differential Shifting

A logic one is transferred to the host by ensuring that the +Data line is driven over 2.8 volts whist the -Data is driven below 0.3 volts. A logic zero is transferred to the host by ensuring that the -Data line is greater than 2.8 volts and the +Data is less than 0.3 volts.

4.12.4 USB NRZI Encoding

The differential shifting is encoded using a non-return to zero inverted (NRZI) encoding technique. Logic one is represented with no change in the transmission level whilst a logic zero is represented by a change in the transition level. Figure 4-20 shows a typical data stream and the NRZI encoded equivalent.

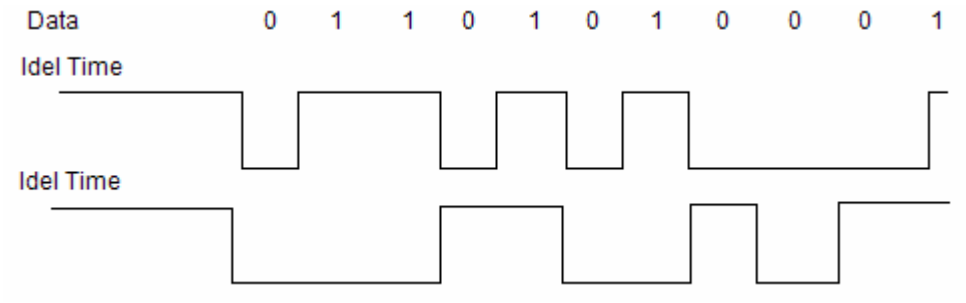


Figure 4-20: NRZI Encoding

4.12.5 Bit Stuffing

Figure 4-20 shows, by only causing a transition only on the logic zero, the bandwidth required to transmit can be significantly reduced, however if a transmission of a long stream of logic ones is required there will be no activity on the transmit line. This inactivity on the transmission line can lead to the transmitter and receiver clocks becoming un-synchronised and data becoming corrupted. To eliminate this synchronisation problem a logic zero is stuffed into the original data stream before the NRZI encoding is done. This stuffed logic zero is used to ensure that the transmission line will always toggle after the seventh bit is sent. This toggling is used to provide a method of synchronisation in the transmitter and receiver. Figure 4-21 shows the flow chart for the bit stuffing process.

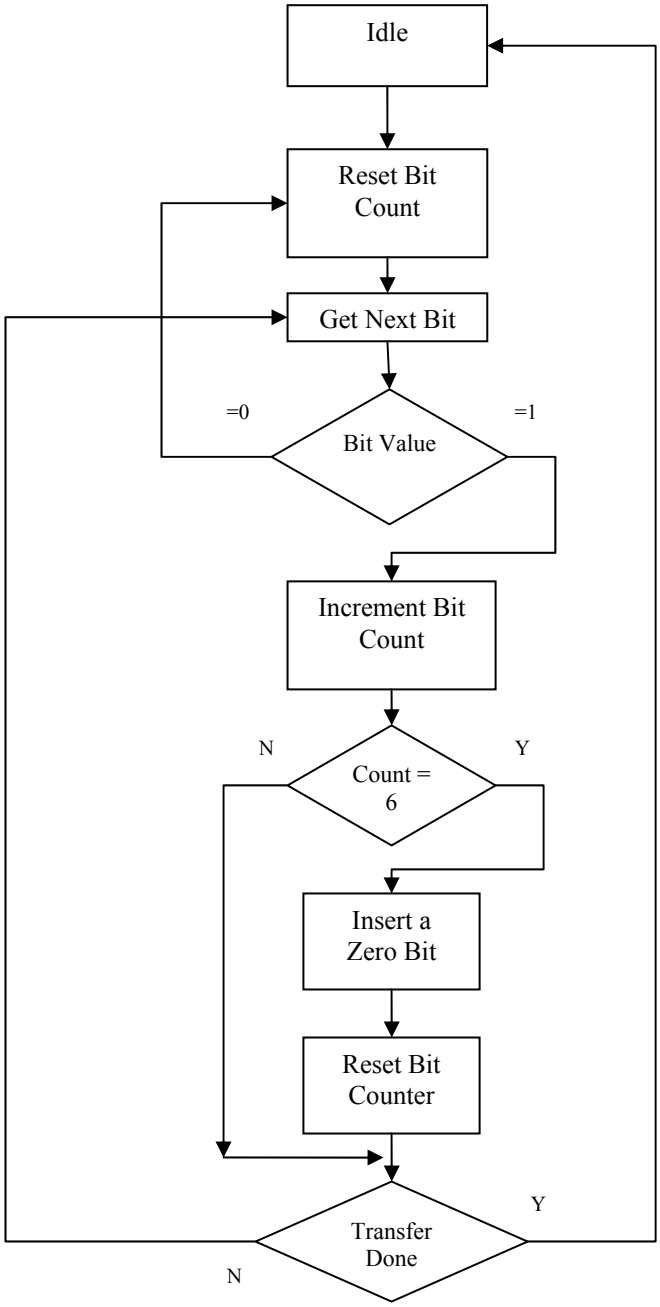


Figure 4-21: Flow Chart Bit Stuffing

4.12.6 Cyclic Redundancy Checking

Cyclic Redundancy Checking (CRC) error checks are used, using a five bit or a 16-bit algorithm. The USB uses the traditional acknowledge (ACK) and no acknowledgment (NAK) to indicate whether the transfer from source to destination is error free. If the transfer resulted in a CRC error, the packet is resent over and over until it is received correctly.

4.12.7 Pin Identification

The USB module is a 32 pin dual in line package (DIL) that provides all the necessary architecture required to interface an eight bit parallel bus structure to a USB interface, as shown in Figure 4-22.

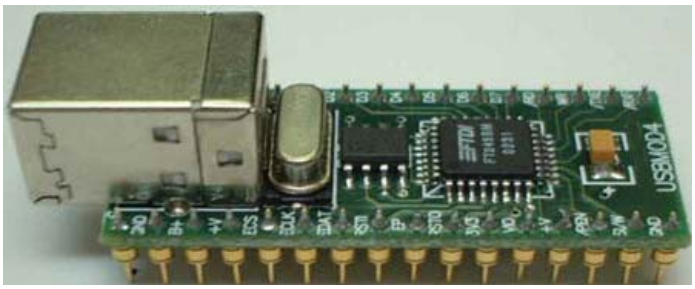


Figure 4-22: USB Interface Module

The parallel interfacing to the USB module is achieved through normal TTL switching logic. The USB module can be treated the same as a single memory mapped device, where data is written directly to that device. Data received by the USB module is latched into the FIFO transmission buffer by toggling the write pin, once the data is stored in the memory. It is then encapsulated into the standard USB

protocol format prior transmission to the host computer. Table 4-6 details the functionality of each pin.

PIN #	SIGNAL	TYPE	DESCRIPTION
1	G	PWR	Device – ground supply pin
2	GND	PWR	Device – ground supply pin
3	B+	PWR	USB bus power
4	+V	PWR	Device - +4.4 volt to +5.25 volt power supply pin note: no external voltage is required when bus powered.
5	ECS	I/O	EEPROM – chip select
6	ECLK	I/O	EEPROM – clock
7	EDAT	OUT	EPPROM– data i/o
8	RSTI	IN	Can be used by external device to reset chip. if not required tie to VCC.
9	EP*	IN	Enumeration power connected to RSTO for bus powered operation.
10	RSTO	OUT	Output of the internal reset generator stays high impedance for ~2ms after VCC >3.5v whilst the internal clock starts up. Taking reset# low will also force RSTOUT# to go high impedance. RSTOUT# is not affected by a USB bus reset.
11	3V3	OUT	3.3 volt output from the integrated L.D.O. regulator this pin is decoupled to GND using a 33nf ceramic capacitor in close proximity to the device pin. its prime purpose is to provide the internal 3.3v supply to the USB transceiver cell and the RSTO pin. a small amount of current (<=5ma) can be drawn from this pin to power external 3.3v logic if required.

PIN #	SIGNAL	TYPE	DESCRIPTION
12	VIO**	PWR	+3.0 volt to +5.25 volt VCC to the FIFO interface pins 10..12,14..16 and 18..25. When interfacing with 3.3v external logic connect the VIO to the 3.3v supply of the external logic, otherwise connect to the +V to drive out at 5v CMOS level.
13	+V	PWR	Device - +4.4 volt to +5.25 volt Power Supply Pin NOTE: No external Voltage is required when Bus Powered.
14	/PEN	OUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to the external logic using a P-Channel Logic Level MOSFET switch. Enables the Interface Pull-Down Option in EEPROM when using the /PEN pin in this way.
15	SI/W	IN	The Send Immediate /WakeUp signal combines two functions on a single pin. If the USB is in suspend mode (/PEN=1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wakeup the Host PC. During normal operations (PEN=0), if this pin is strobed low then any data in the device RX buffer will be sent out over the USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimise USB transfer speed for some applications. Tie this pin high if not used.
16	GND	PWR	Device – ground supply pin

PIN #	SIGNAL	TYPE	DESCRIPTION
17	/RXF	OUT	When high, do not read data from FIFO. When low, there is data available in the FIFO, which can be read by strobing the /RD low then high again.
18	/TXE	OUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high then low.
19	WR	IN	Writes the Data Byte on D0..D7 into the Transmit FIFO Buffer when WR goes from high to low.
20	/RD	IN	Enables Current FIFO Data Byte on D0-D7 when low. Fetches the next FIFO Data Byte (if available) from the receive FIFO Buffer when /RD goes from low to high.
21	D7	I/O	Bi-directional data bus bit #7
22	D6	I/O	Bi-directional data bus bit #6
23	D5	I/O	Bi-directional data bus bit #5
24	D4	I/O	Bi-directional data bus bit #4
25	D3	I/O	Bi-directional data bus bit #3
26	D2	I/O	Bi-directional data bus bit #2
27	D1	I/O	Bi-directional data bus bit #1
28	D0	I/O	Bi-directional data bus bit #0
29	GND	PWR	Device – ground supply pin
30	D-	I/O	USB data signal minus
31	D+	I/O	USB data signal plus
32	G	PWR	Device – ground supply pin

Table 4-6: Pin Identification USB Module

4.12.8 FT245DM Block Diagram

Figure 4-23 shows a simple block diagram and description of the internal structure of the USB module used in the audio interface.

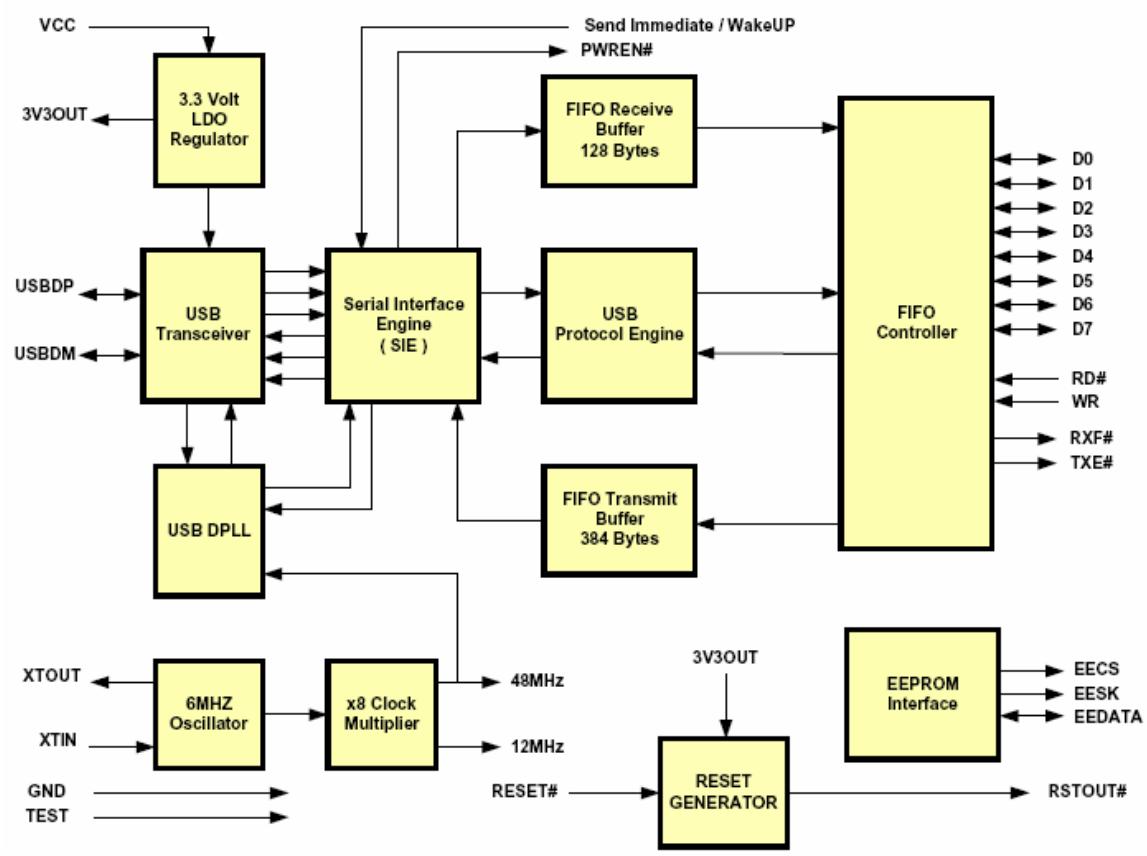


Figure 4-23: USB Block Diagram

4.12.9 USB Transceiver

The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver provide USB data in.

4.12.10 Serial Interface Engine

The serial interface engine (SIE) block performs the parallel to serial and the serial to parallel conversion of the USB data. In accordance with the USB 2.0 specifications, it performs bit stuffing / un-stuffing and CRC checking on the USB data stream.

4.12.11 USB Protocol Engine

The USB protocol engine manages the data stream from the SIE to the USB control endpoint. It handles the low level USB protocol requests, generated by the USB host controller, and the commands for controlling the functional parameters of the FIFO.

4.12.12 Receive Buffer

Data sent from the USB host and stored in the receive buffer, data is removed from the buffer by reading the FIFO contents using the RD#.

4.12.13 FIFO Transmit Buffer

Data written into the FIFO using WR# is stored in the FIFO transmit buffer. The host removes data from the FIFO buffer by sending a USB request command.

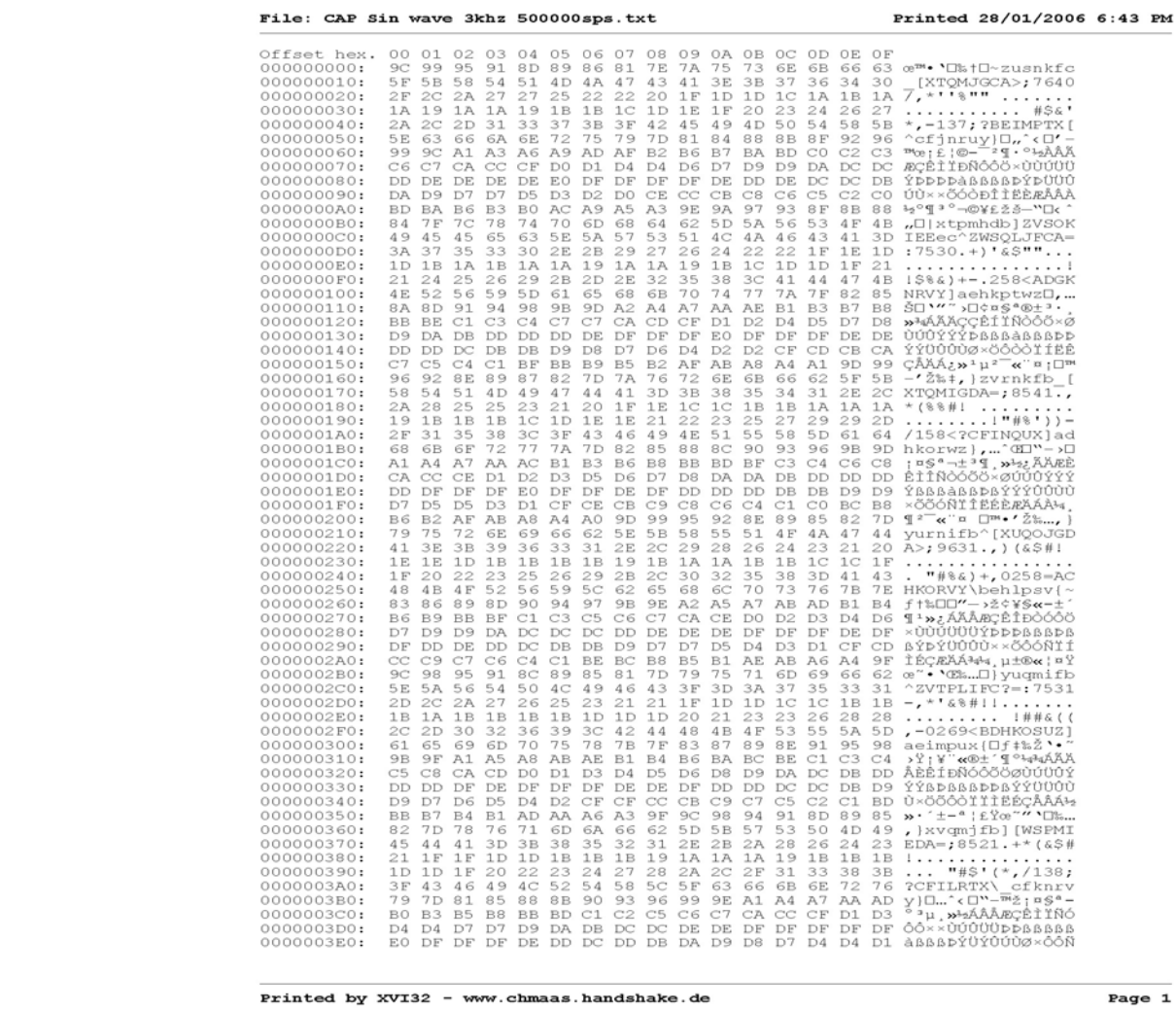
4.12.14 FIFO Controller

The FIFO Controller handles the transfer of data between the external FIFO interface pins and the FIFO transmit and receive buffer.

5.0 TEST RESULTS

The serial USB raw data was captured from the audio interface with a terminal program, this program is available for downloading from the internet called ‘realterm’, which can be found at the web site http://realterm.sourceforge.net/ for free.

Realterm is a terminal program specially designed for capturing, controlling, and debugging binary data streams from the virtual communication port, and saved as a TXT file for later debugging as shown in Figure 5-1.



```
File: CAP Sin wave 3khz 500000sps.txt                    Printed 28/01/2006 6:43 PM

Offset hex.  00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
00000000:  9C 99 95 91 8D 89 86 81 7E 7A 75 73 6E 6B 66 63 œ™•‘□‰†□~zusnkfc
00000010:  5F 5B 58 54 51 4D 4A 47 43 41 3E 3B 37 36 34 30 _[XTQMJGCA>;7640
00000020:  2F 2C 2A 27 27 25 22 22 20 1F 1D 1D 1C 1A 1B 1A /,*''%"" ........
00000030:  1A 19 1A 1A 19 1B 1B 1C 1D 1E 1F 20 23 24 26 27 ........... #$&'
00000040:  2A 2C 2D 31 33 37 3B 3F 42 45 49 4D 50 54 58 5B *,-137;?BEIMPTX[
00000050:  5E 63 66 6A 6E 72 75 79 7D 81 84 88 8B 8F 92 96 ^cfjnruy}□„ˆ‹□’–
00000060:  99 9C A1 A3 A6 A9 AD AF B2 B6 B7 BA BD C0 C2 C3 ™œ¡£¦©¯²¶·º½ÀÂÃ
00000070:  C6 C7 CA CC CF D0 D1 D4 D6 D7 D9 D9 DA DC DC ÆÇÊÌÏÐÑÔÖ×ÙÙÚÜÜ
00000080:  DD DE DE DE DE E0 DF DF DF DF DE DD DE DC DC DB ÝÞÞÞÞàßßßßßÞÝÞÜÜÛ
00000090:  DA D9 D7 D7 D5 D3 D2 D0 CE CC CB C8 C6 C5 C2 C0 ÚÙ××ÕÓÒÐÎÌËÈÆÅÂÀ
000000A0:  BD BA B6 B3 B0 AC A9 A5 A3 9E 9A 97 93 8F 8B 88 ½º¶³°¬©¥£žš—"□‹ˆ
000000B0:  84 7F 7C 78 74 70 6D 68 64 62 5D 5A 56 53 4F 4B „□|xtpmhdb]ZVSOK
000000C0:  49 45 45 65 63 5E 5A 57 53 51 4C 4A 46 43 41 3D IEEec^ZWSQLJFCA=
000000D0:  3A 37 35 33 30 2E 2B 29 27 26 24 22 22 1F 1E 1D :7530.+)'&$""...
000000E0:  1D 1B 1A 1B 1A 1A 19 1A 19 1B 1C 1D 1D 1F 21 ..............!
000000F0:  21 24 25 26 29 2B 2D 2E 32 35 38 3C 41 44 47 4B !$%&)+-.258<ADGK
00000100:  4E 52 56 59 5D 61 65 68 6B 70 74 77 7A 7F 82 85 NRVY]aehkptwz□,…
00000110:  8A 8D 91 94 98 9B 9D A2 A4 A7 AA AE B1 B3 B7 B8 Š□‘”˜›□¢¤§ª®±³·¸
00000120:  BB BE C1 C3 C4 C7 C7 CA CD CF D1 D2 D4 D5 D7 D8 »¾ÁÃÄÇÇÊÍÏÑÒÔÕ×Ø
00000130:  D9 DA DB DD DD DD DE DF DF DF E0 DF DF DF DE DE ÙÚÛÝÝÝÞßßßßàßßßÞÞ
00000140:  DD DD DC DB DB D9 D8 D7 D6 D4 D2 D2 CF CD CB CA ÝÝÜÛÛÙØ×ÖÔÒÒÏÍËÊ
00000150:  C7 C5 C4 C1 BF BB B9 B5 B2 AF AB A8 A4 A1 9D 99 ÇÅÄÁ¿»¹µ²¯«¨¤¡□™
00000160:  96 92 8E 89 87 82 7D 7A 76 72 6E 6B 66 62 5F 5B –’Ž‰‡‚}zvrnkfb_[
00000170:  58 54 51 4D 49 47 44 41 3D 3B 38 35 34 31 2E 2C XTQMIGDA=;8541.,
00000180:  2A 28 25 25 23 21 20 1F 1E 1C 1C 1B 1B 1A 1A 1A *(%%#! ..........
00000190:  19 1B 1B 1B 1C 1D 1E 1E 21 22 23 25 27 29 29 2D ........!"#%'))-
0000001A0:  2F 31 35 38 3C 3F 43 46 49 4E 51 55 58 5D 61 64 /158<?CFINQUX]ad
0000001B0:  68 6B 6F 72 77 7A 7D 82 85 88 8C 90 93 96 9B 9D hkorwz},…ˆŒ□‘”–›□
0000001C0:  A1 A4 A7 AA AC B1 B3 B6 B8 BB BD BF C3 C4 C6 C8 ¡¤§ª¬±³¶¸»½¿ÃÄÆÈ
0000001D0:  CA CC CE D1 D2 D3 D5 D6 D7 D8 DA DA DB DD DD DD ÊÌÎÑÒÓÕÖ×ØÚÚÛÝÝÝ
0000001E0:  DD DF DF DF E0 DF DF DE DF DD DD DD DB DB D9 D9 ÝßßßàßßÞßÝÝÛÛÛÙÙ
0000001F0:  D7 D5 D5 D3 D1 CF CE CB C9 C8 C6 C4 C1 C0 BC B8 ×ÕÕÓÑÏÎËÉÈÆÄÁÀ¼¸
00000200:  B6 B2 AF AB A8 A4 A0 9D 99 95 92 8E 89 85 82 7D ¶²¯«¨¤ □™•’Ž‰…‚}
00000210:  79 75 72 6E 69 66 62 5E 5B 58 55 51 4F 4A 47 44 yurnifb^[XUQOJGD
00000220:  41 3E 3B 39 36 33 31 2E 2C 29 28 26 24 23 21 20 A>;9631.,)(&$#!
00000230:  1E 1E 1D 1B 1B 1B 1B 19 1B 1A 1A 1B 1B 1C 1C 1F ................
00000240:  1F 20 22 23 25 26 29 2B 2C 30 32 35 38 3D 41 43 . "#%&)+,0258=AC
00000250:  48 4B 4F 52 56 59 5C 62 65 68 6C 70 73 76 7B 7E HKORVY\behlpsv{~
00000260:  83 86 89 8D 90 94 97 9B 9E A2 A5 A7 AB AD B1 B4 ƒ†‰□□”–›ž¢¥§«±´
00000270:  B6 B9 BB BF C1 C3 C5 C6 C7 CA CE D0 D2 D3 D4 D6 ¶¹»¿ÁÃÅÆÇÊÎÐÒÓÔÖ
00000280:  D7 D9 D9 DA DC DC DC DD DE DE DE DF DF DF DE DF ×ÙÙÚÜÜÜÝÞÞÞßßßßß
00000290:  DF DD DE DD DC DB DB D9 D7 D7 D5 D4 D3 D1 CF CD ßÝÞÝÜÛÛÙ××ÕÔÓÑÏÍ
0000002A0:  CC C9 C7 C6 C4 C1 BE BC B8 B5 B1 AE AB A6 A4 9F ÌÉÇÆÄÁ¾¼¸µ±®«¦¤Ÿ
0000002B0:  9C 98 95 91 8C 89 85 81 7D 79 75 71 6D 69 66 62 œ˜•‘Œ‰…□}yuqmifb
0000002C0:  5E 5A 56 54 50 4C 49 46 43 3F 3D 3A 37 35 33 31 ^ZVTPLIFC?=:7531
0000002D0:  2D 2C 2A 27 26 25 23 21 21 1F 1D 1D 1C 1C 1B 1B -,*'&%#!!........
0000002E0:  1B 1A 1B 1B 1B 1B 1D 1D 1D 20 21 23 23 26 28 28 ......... !##&((
0000002F0:  2C 2D 30 32 36 39 3C 42 44 48 4B 4F 53 55 5A 5D ,-0269<BDHKOSUZ]
00000300:  61 65 69 6D 70 75 78 7B 7F 83 87 89 8E 91 95 98 aeimpux{□ƒ‡‰Ž‘•˜
00000310:  9B 9F A1 A5 A8 AB AE B1 B4 B6 BA BC BE C1 C3 C4 ›Ÿ¡¥¨«®±´¶ºº¼¾ÁÃÄ
00000320:  C5 C8 CA CD D0 D1 D3 D4 D5 D6 D8 D9 DA DC DB DD ÅÈÊÍÐÑÓÔÕÖØÙÚÜÛÝ
00000330:  DD DD DF DE DF DF DE DE DF DD DD DC DC DB D9 ÝÝßÞßßßÞÞßÝÝÜÜÛÙ
00000340:  D9 D7 D6 D5 D4 D2 CF CF CC CB C9 C7 C5 C2 C1 BD Ù×ÖÕÔÒÏÏÌËÉÇÅÂÁ½
00000350:  BB B7 B4 B1 AD AA A6 A3 9F 9C 98 94 91 8D 89 85 »·´±ª¦£Ÿœ˜”‘□‰…
00000360:  82 7D 78 76 71 6D 6A 66 62 5D 5B 57 53 50 4D 49 ‚}xvqmjfb][WSPMI
00000370:  45 44 41 3D 3B 38 35 32 31 2E 2B 2A 28 26 24 23 EDA=;8521.+*(&$#
00000380:  21 1F 1F 1D 1D 1B 1B 1B 19 1A 1A 1A 19 1B 1B 1B !...............
00000390:  1D 1D 1F 20 22 23 24 27 28 2A 2C 2F 31 33 38 3B ... "#$'(*,/138;
0000003A0:  3F 43 46 49 4C 52 54 58 5C 5F 63 66 6B 6E 72 76 ?CFILRTX\_cfknrv
0000003B0:  79 7D 81 85 88 8B 90 93 96 99 9E A1 A4 A7 AA AD y}□…ˆ‹□‘”–™š¡¤§ª
0000003C0:  B0 B3 B5 B8 BB BD C1 C2 C5 C6 C7 CA CC CF D1 D3 °³µ¸»½ÁÂÅÆÇÊÌÏÑÓ
0000003D0:  D4 D4 D7 D7 D9 DA DB DC DC DE DE DF DF DF DF ÔÔ××ÙÚÛÜÜÞÞßßßßß
0000003E0:  E0 DF DF DF DE DD DC DD DB DA D9 D8 D7 D4 D4 D1 àßßßÞÝÜÝÛÚÙØ×ÔÔÑ

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Figure 5-1: Raw Data as a TXT File

The raw data captured by realterm can be imported and the original audio signal reconstructed with an audio program This is also available free from http://audacity.sourceforge.net/ and is called audacity.

Three audio frequencies were selected for analysis, as this will cover the lower, mid and upper audio range of the interface bandwidth filters, as shown in Table 5-1.

Test No	Audio Input	Input Frequency	Audio Output	Amplifier Gain	Output Frequency	Plot Figure
1	1 Volt	3 KHz	1.5Volt	1.5 dB	3 KHz	Fig 29
2	1Volt	47 KHz	1.5Volt	1.5 dB	47 KHz	Fig 30
3	1Volt	81 KHz	1.5Volt	1.5 dB	81 KHz	Fig 31

Table 5-1: Test Results

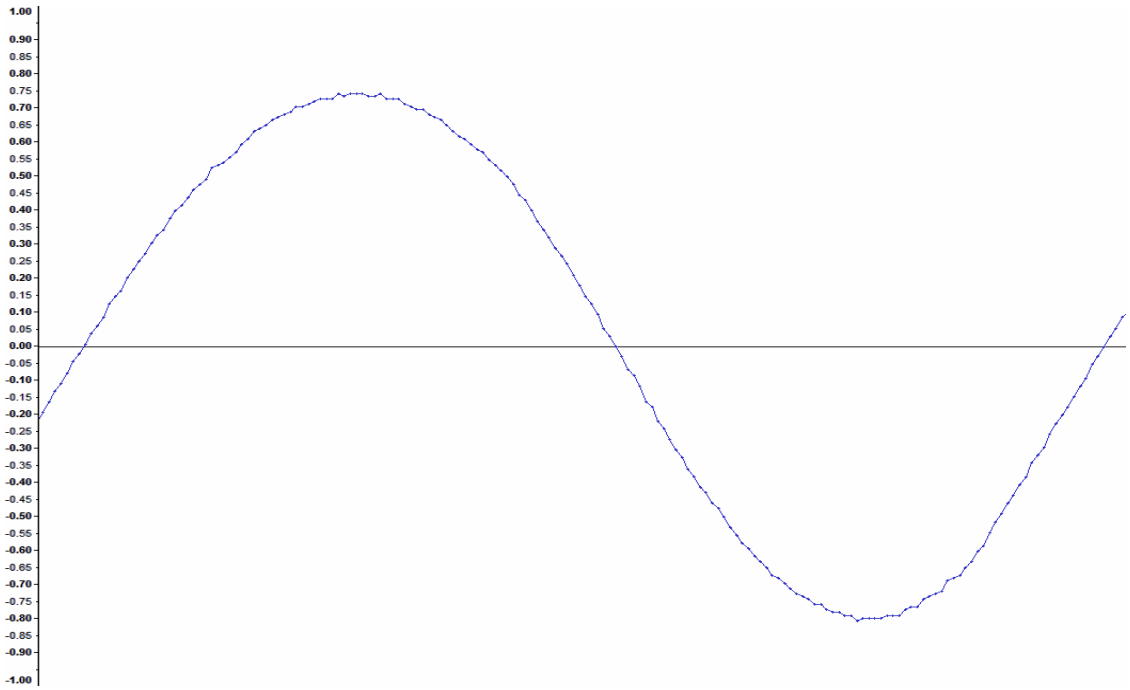

Figure 5-2: 3 KHz Sin Wave Captured at 500Ksps

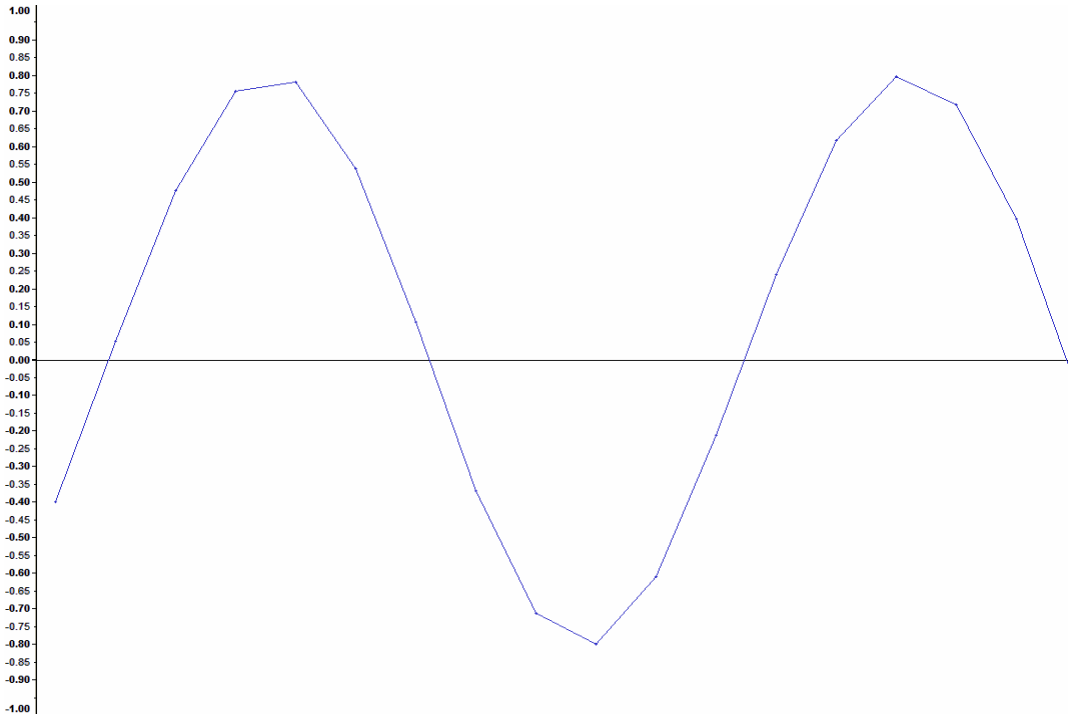

Figure 5-3: 47 KHz Sin Wave Captured at 500Ksps

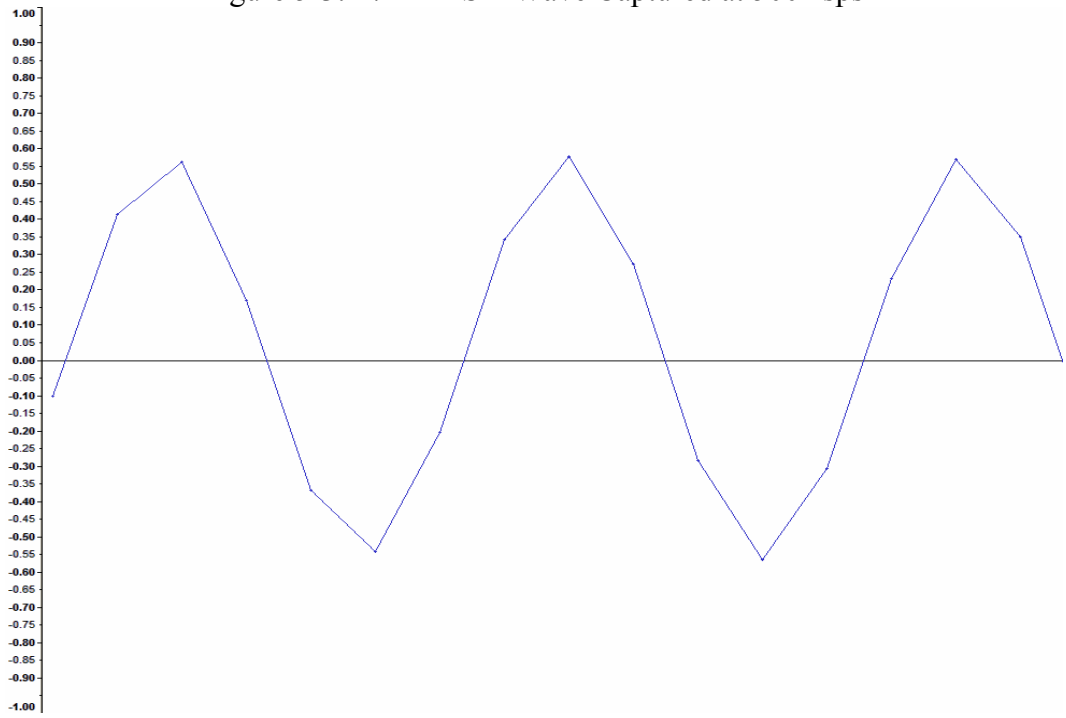

Figure 5-4: 81 KHz Sin Wave Captured at 500Ksps

6.0 CONCLUSION

It is not obvious that an exact reconstruction of an analogue signal is possible, since an analogue waveform is a continuously moving signal that has a finite number of points that can be sampled. This is achieved by using the Nyquist sampling theorem which states, provided you can sample at twice the frequency rate required there will be no loss in the original signal information.

It is important to note that sampling at a rate lower than twice the required frequency results in a phenomenon called aliasing, whereby the resulting digital signal lacks sufficient information to reconstruct the original waveform which will lead to a noisy recording. Once aliasing has been introduced into the digitised signal it is impossible to remove the noisy recording from the digitised audio signal.

Audible signals that humans can hear lie in the range of 20 Hz to 20 KHz. Voice audio on the other hand is limited to even a narrower band of frequencies in the range of 150Hz to 6 KHz, although there will be very little audio at this upper range. In order to reconstruct exactly the original analogue signal a sample rate of at least 12ksps, as stated in the sampling theorem is required. Since a factor of 20 is being used in this audio interface, it is recommended to sample at a minimum sample rate of 240ksps of which the audio interface will then sample at a maximum of 500ksps.

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8.0 APPENDIX A PART LISTING

Table 8-1 contains a full part listing of components, suppliers and suppliers part numbers used to produce the audio interface printed circuit board.

PART ID	DEVICE	SUPPLIER	PART No
U1	SPG6840BN	Farnell	170-680
U2	TLV2772	RS	356-8969
U2 Socket	8 Way Interface Socket DIP - SOIC	RS	158-2878
U3	SV-4BL	RS	501-6628
U4	PST5101	Farnell	311-4892
U5	SN74121	RS	305-591
U6	SN74LS14	RS	307-547
U7	SN74LS132	RS	309-133
U8	AD7821	RS	310-830
U9	CY7C466A	RS	469-6330
U9 Socket	32 PLCC Socket Though Hole Mounting	Farnell	233-043
U10	USB Mod4 (ELEXOL)	Dontronic	MOB4
U11	DS1233	RS	248-3003
U12	50A-10151	RS	299-200
SW1	6 Channel	RS	291-1025
T1	BC547	RS	296-087
SW2	Switch Toggle (optional)	RS	448-1172
J1	Phono Socket RCA (PCB mount) Phono Socket RCA (Case mount)	Farnell Farnell	152-396 414-9774
J2	2.1mm Power Jack PCB	RS	486-662
R1	1k62 / 0.25W	RS	165-961
R2	1k62 / 0.25W	RS	165-961
R3	1k62 / 0.25W	RS	165-961
R4	1k62 / 0.25W	RS	165-961
R5	4k7 / 0.25W	RS	131-334
R6	4k7 / 0.25W	RS	131-334

PART ID	DEVICE	SUPPLIER	PART No
R7	4k7 / 0.25W	RS	131-334
R8	1k / 0.25w	RS	131-225
R9	10k / 0.25w	RS	131-378
R10	220k / 0.25w	RS	131-536
R11	3k3 / 0.25W	RS	131-312
R12	10k / 0.25w	RS	131-378
R13	10k / 0.25w	RS	131-378
R14	10k / 0.25w	RS	131-378
R15	4k7 / 0.25W	RS	131-334
R16	10k / 0.25w	RS	131-378
R17	4k7 / 0.25W	RS	131-334
R18	220k / 0.25w (optional)	RS	131-536
R19	1k / 0.25w	RS	131-225
R20	1k / 0.25w	RS	131-225
R21	10k / 0.25w	RS	131-378
R22	1k / 0.25w	RS	131-225
D1	1N4001	RS	261-148
Z1	BZX79C2V4A26A	RS	446-8589
C1	1uF	RS	228-6846
C2	100uF	RS	228-6903
C3	0.1uF	RS	312-1469
C4	0.1uF	RS	312-1469
C5	0.1uF	RS	312-1469
C6	0.1uF	RS	312-1469
C7	0.1uF	RS	312-1469
C8	47uF	RS	312-1481
C9	0.1uF	RS	312-1469
C10	22pF	RS	264-4668
C11	0.1uF	RS	312-1469
C12	0.1uF	RS	312-1469
C13	0.1uF	RS	312-1469
C14	0.1uF	RS	312-1469

PART ID	DEVICE	SUPPLIER	PART No
C15	0.1uF	RS	312-1469
C16	0.1uF	RS	312-1469
C17	0.1uF	RS	312-1469
C18	0.1uF	RS	312-1469
C19	0.1uF	RS	312-1469
P1	10k Trimmer 25T	Altronic	R2382A
P2	50k Trimmer 25T	Altronic	R2386A
P3	100k Trimmer 25T	Altronic	R2388A
PCB	Blank printed circuit board	CadLink	8588 Rev1
EN1	Enclosure (if required)	Farnell	427-2833
Power Supply	Plug Pack 12vdc 500mA	Altronics	M9265
Audio Cable	RCA to RCA Audio cable	Altronics	P6201
USB Cable	Type A male to mini male	Altronics	P1893

Table 8-1: Audio Interface Component Listing

9.0 APPENDIX B CIRCUIT SCHEMATIC

Figure 9-1 provides the schematic for the audio interface.

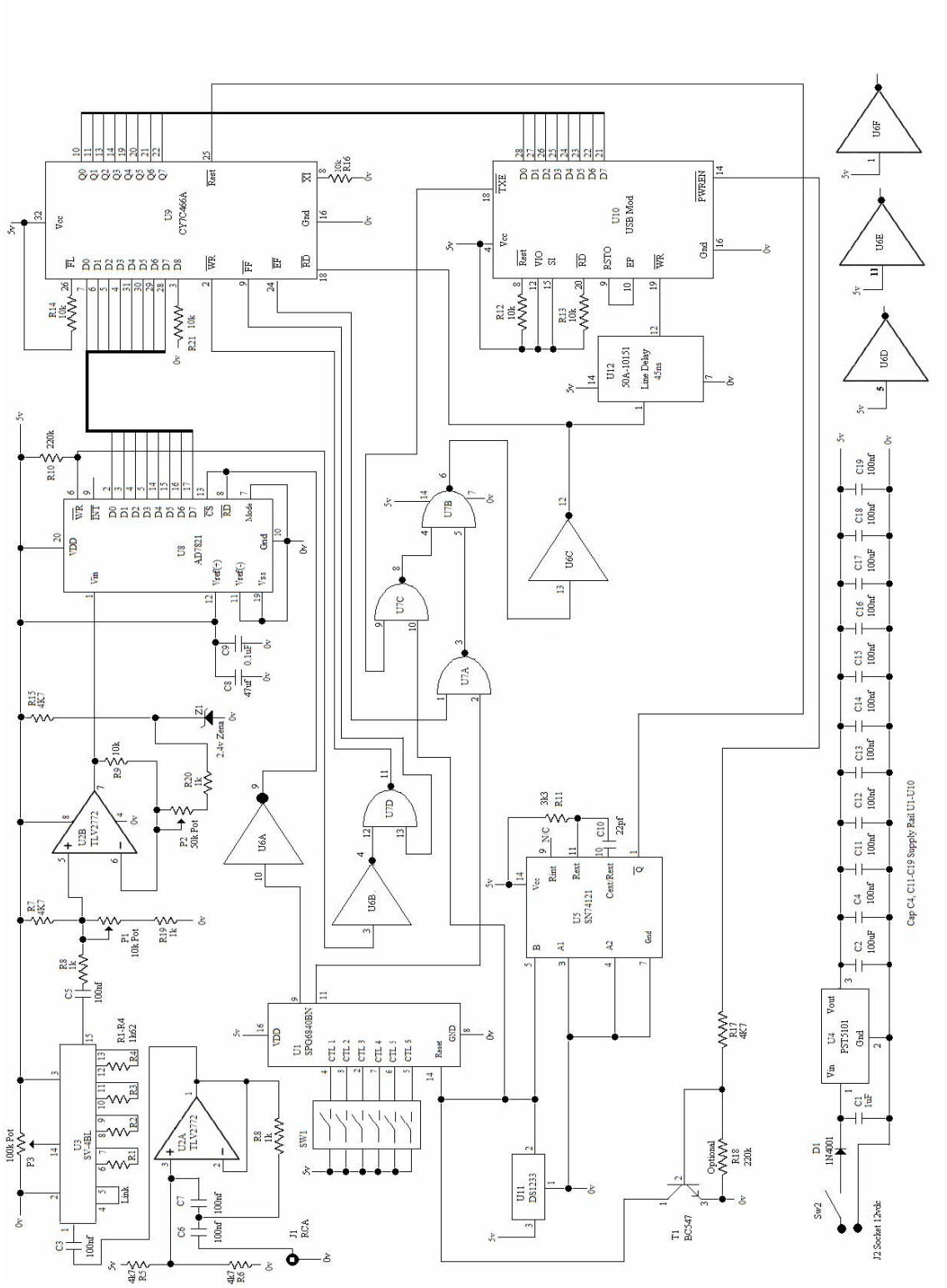

Figure 9-1: Audio Interface Schematic

10.0 APPENDIX C PCB LAYOUT

Figure 10-1 provides the component layout, whilst Figures 10-2 and Figures 10-3 detail the copper tracks and earth matting for the audio interface.

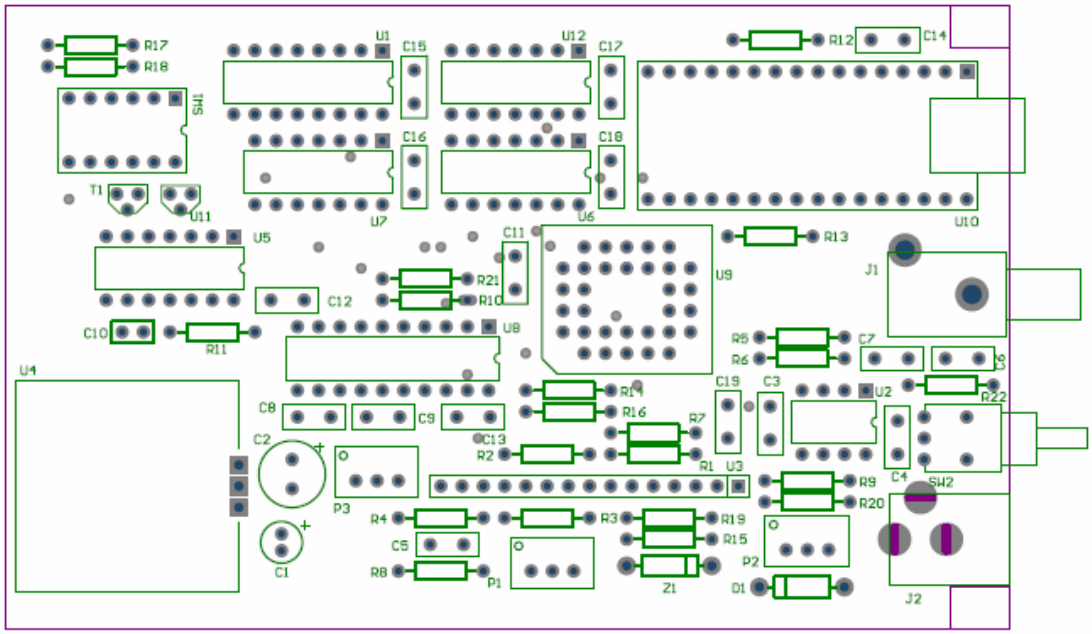

Figure 10-1: PCB Layout

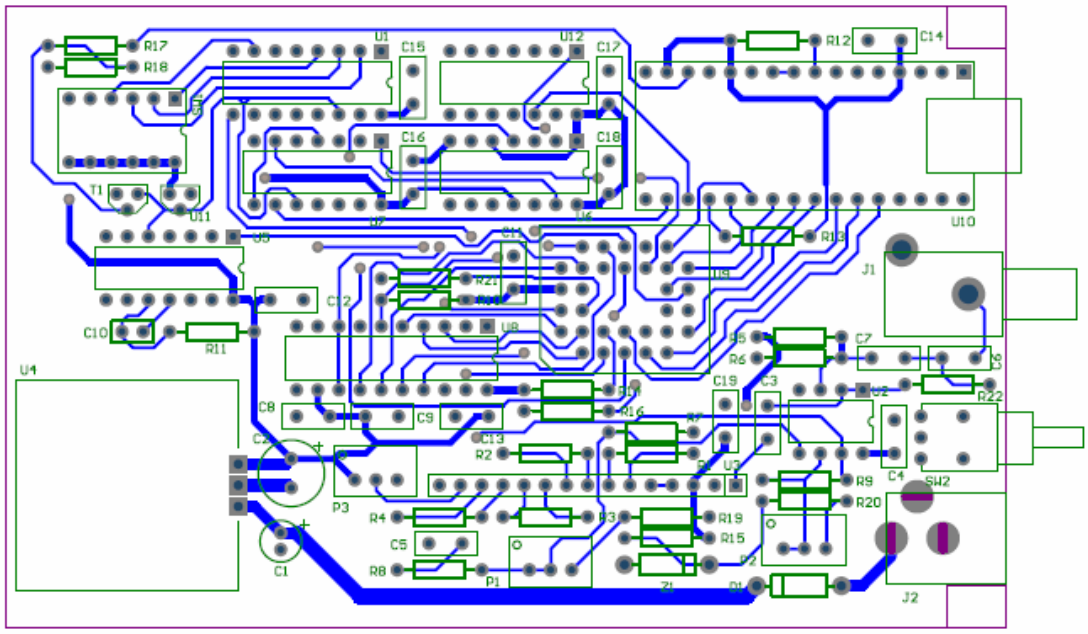

Figure 10-2: Bottom View of Track Layout

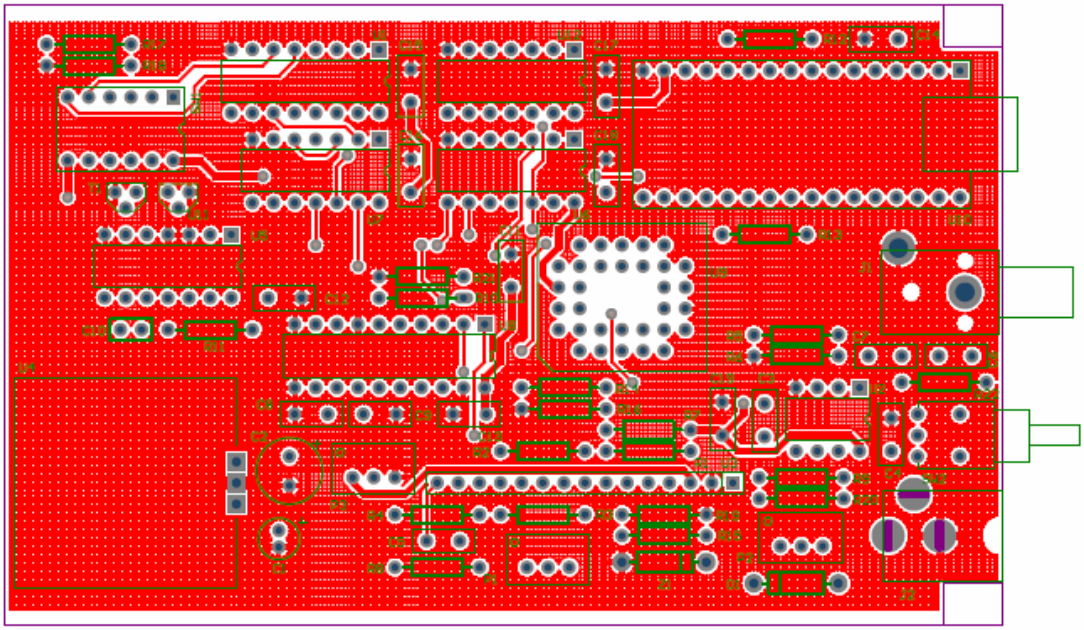

Figure 10-3: Top View of Earth Mat and Track Layout

11.0 APPENDIX D PCB TRACK MODIFICATION

Figure 11-4 shows the modification required to the PCB due to tracking errors, all the tracking errors have since been rectified in the latest revision.

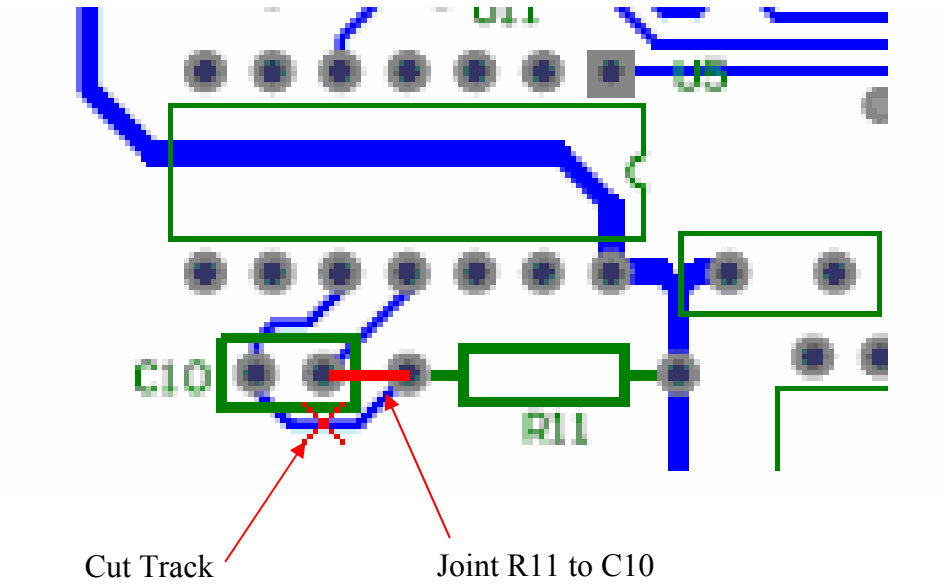

Figure 11-1: Tracking Error Modification

The USB interface can be powered in two modes of operation, bus powered or self powered. By default the USB interface is supplied by the manufacturer to operate in bus powered mode. The audio interface requires the USB module to be configured to operate in self powered mode, therefore ferrite bead FB1 is to be removed from the USB module, as shown in Figure 11-2.

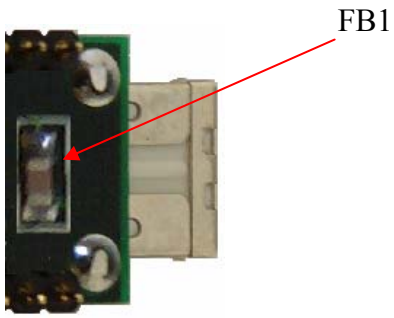

Figure 11-2: USBMOD4 Self Powered Link

12.0 APPENDIX E ELECTRICAL SPECIFICATION

Figure 12-1 and Table 12-1 provides the electrical connections and specification for the audio interface.

Figure 12-1: Audio Interface Connections

CONNECTIONS	CHARACTERISTIC	CONDITIONS	MIN	TYPE	MAX	UNITS
Not applicable	Input Current	Over Vin Range	0.13	0.14	0.15	A
Tip Positives Ring Negative	Input Voltage Range	Over Io Range	9.0	12.0	38.0	VDC
Tip Signal Ring Negatives	Audio Level	Over Vin Range	0.19	2.0	2.5	VAC
Pin 2 Data – Pin 3 Data +	USB 2.0	Over Tx Range	N/A	N/A	8.0	Mbps

Table 12-1: Electrical Specification