SPECTRUM DIGITAL INCORPORATED

TMS320C50/TMS320C51 Evaluation Module

Technical Reference

1998 *DSP Development Systems*

TMS320C50/TMS320C51
Evaluation Module
Technical Reference

503481-0001 Rev. C
March 1998

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About This Manual

This document describes the board level operations of the TMS320C50/TMS320C51 evaluation module (EVM). The EVM is based on the Texas Instruments TMS320C50 and TMS320C51Digital Signal Processor.

The TMS320C5X EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C50 and TMS320C51 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C50 will sometimes be referred to as the C50 or C5X.

The TMS320C51 will sometimes be referred to as the C51 or C5X.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320C5X Users Guide
Texas Instruments TMS320 Fixed Point Assembly Language Users Guide
Texas Instruments TMS320 Fixed Point C Language Users Guide
Texas Instruments TMS320 Fixed Point C Source Debugger Users Guide
Texas Instruments TLC320AD55C Data Manual - SLAS085
Texas Instruments TLC320AD55 Evaluation Board Application Report - SLAE11

Chapter 1

Introduction to the TMS320C5X Evaluation Module

This chapter provides you with a description of the TMS32C5X Evaluation Module along with the key features and a block diagram of the circuit board.

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1.0 Overview of the TMS320C5X EVM

The TMS320C5X evaluation module(EVM) is a stand-alone card that lets evaluators examine certain characteristics of the TMS320C50 or TMS320C51 digital signal processor(DSP) to determine if this DSP meets their application requirements. Furthermore, the module is an excellent platform to develop and run software on the C5X family of processors.

The C5X EVM is shipped with a choice of DSPs; the TMS320C50, the TMS320C51, the TMS320BC51, or other pin compatible family members as they become available. The EVM allows full speed verification of C5X code. With at least 544 words of onchip memory, 128K words of onboard memory, onchip/onboard boot flash rom, on chip UART, on board UART, and a TLC320AD55 sigma delta codec the board can solve a variety of problems as shipped. Four expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time a number of optional user interfaces are provided.

1.1 Key Features of the TMS320C5X EVM

The C5X EVM has the following features:

- C50 operating at 40 Mips with 128K words of zero wait state memory
  C51/BC51 operating at 40 Mips
- TLC320AD55 Sigma Delta Codec with RCA Jack input and output
- On board UART with RS232 Drivers
- 32K words on board Flash ROM
- 4 Expansion Connectors
- On board IEEE 1149.1 JTAG Connection for Optional Emulation
- 5 Volt Only Operation

1.2 Functional Overview of the TMS320C5X EVM

Figure 1-1 shows a block diagram of the basic configuration for the C5X EVM. The major interfaces of the EVM include the target ram and rom interface, target UART, analog interface, and expansion interface.

The C5X interfaces to 128K Words of zero wait-state static memory. An external I/O interface supports 65,000 parallel I/O ports and optional high speed synchronous serial port. A Flash Rom is mapped into the global memory interface. RCA jacks provide input and outputs to and from the AD55 sigma delta codec.

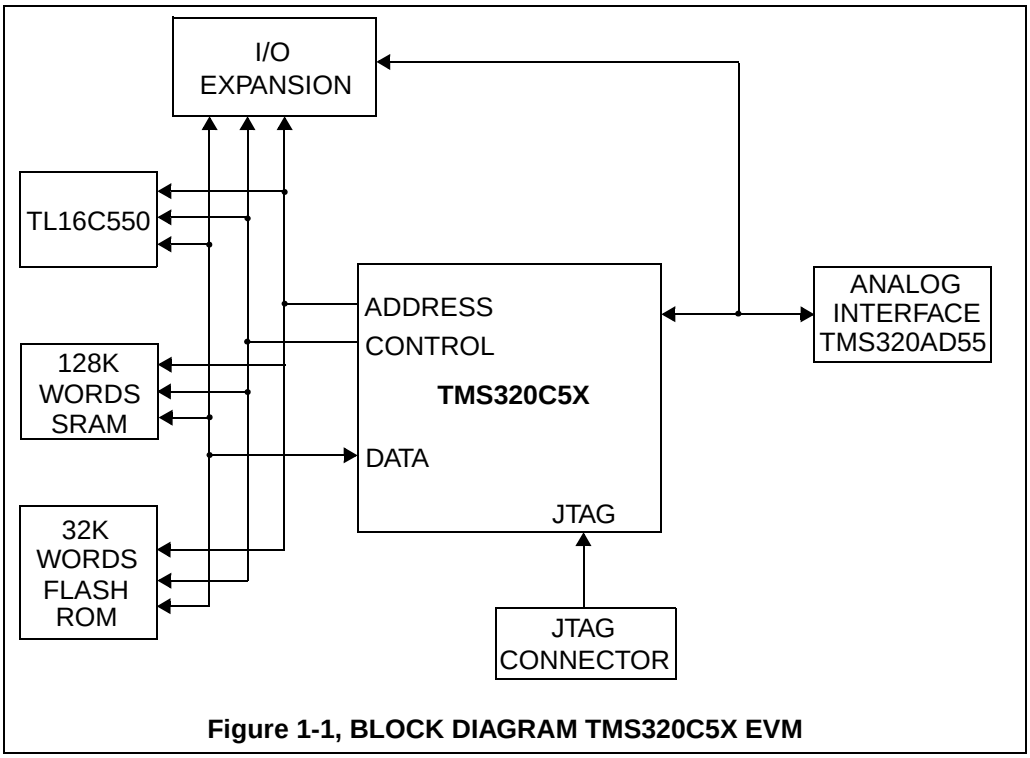

Figure 1-1, BLOCK DIAGRAM TMS320C5X EVM

Chapter 2

Operation of the TMS320C5X Evaluation Module

This chapter describes the operation of the TMS32C5X Evaluation Module along with the key interfaces and an outline of the circuit board.

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2.0 The EVM320C5X Operation

This chapter describes the C5X Evaluation module, its key components, and how they operate. It also provides information on the EVM's various interfaces.The C5X EVM consists of five major blocks of logic.

- C5X memory interface
- Analog Interface
- On board serial interface
- Expansion connector interface
- JTAG interface

2.1 The TMS320C5X EVM Board

The EVM320C5X is a 3U sized board which is powered by an external 5 Volt only power supply. Figure 2-1 shows the layout of the C5X EVM.

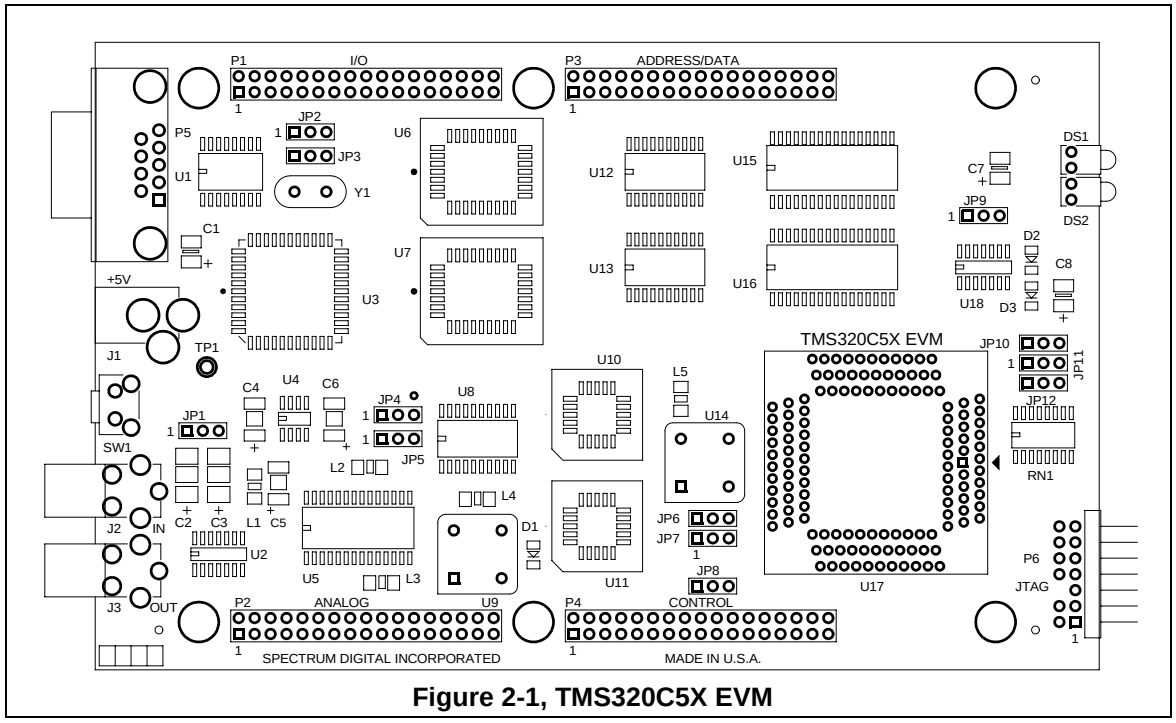


Figure 2-1, TMS320C5X EVM

2.1.1 Power Connector, J1

The C5X is powered by a 5 Volt only power supply which is available with the module. The board requires 750 milliamps. The power is supplied via 2 millimeter jack J1. If expansion boards are connected to the module a higher amperage power supply may be necessary.

2.2 TMS320C5X Memory Interface

The EVM includes 64k words of zero wait-state program ram memory and 64k words of zero wait-state data ram memory, providing a total of 128 k words of off chip static ram. The board also features 2 external 32K byte flash roms. These roms are located in the global memory space and can be used to boot load programs with the onchip boot loader or can be mapped in program space and copied into ram and disabled with the pseudo boot loader. A jumper (JP11) is connected to the MC/MP pin and allows users to enable or disable the on chip bootloader at power up (C50, BC51 only)

Figure 2-2 and 2-3 show the EVM's memory map. It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your EVM card please refer to Texas Instruments TMS320C5X Users Guide. Futhermore, it is important to take into account that external memory is affected by wait-states. Wait state generation is done with the PDWSR, CWSR, and IOWSR on chip wait-state generation registers and off chip with the ready signal. To obtain zero waitstate memory in both the program and data memory spaces the on-chip wait-state generators must be appropriately programmed. The board powers up with 7 wait-states. The EVM board does not generate wait states via the ready signal for external program and data memory accesses. Only external I/O accesses to on-board peripherals generate a not ready signal. The I/O Wait States should not be set to less than 3 in the IOSWR Register.

The memory map for the EVM with a C50 DSP is shown below:

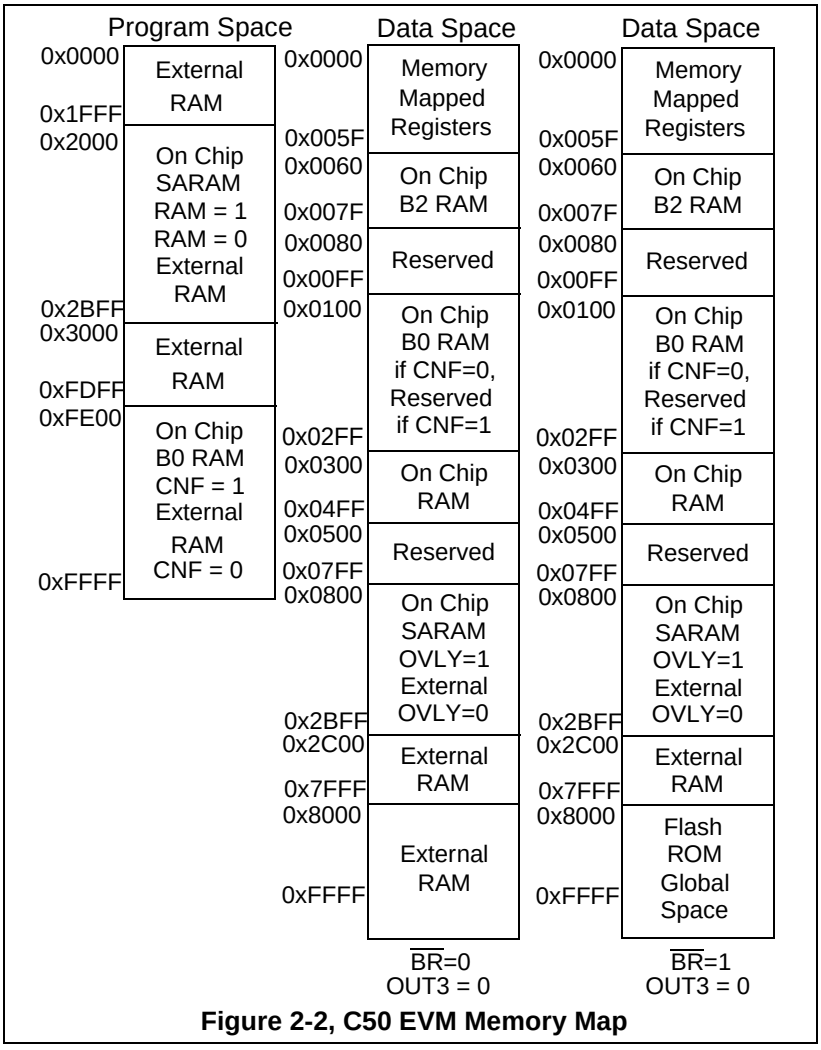


Figure 2-2, C50 EVM Memory Map

The memory map for the EVM with a C51 DSP is shown below:

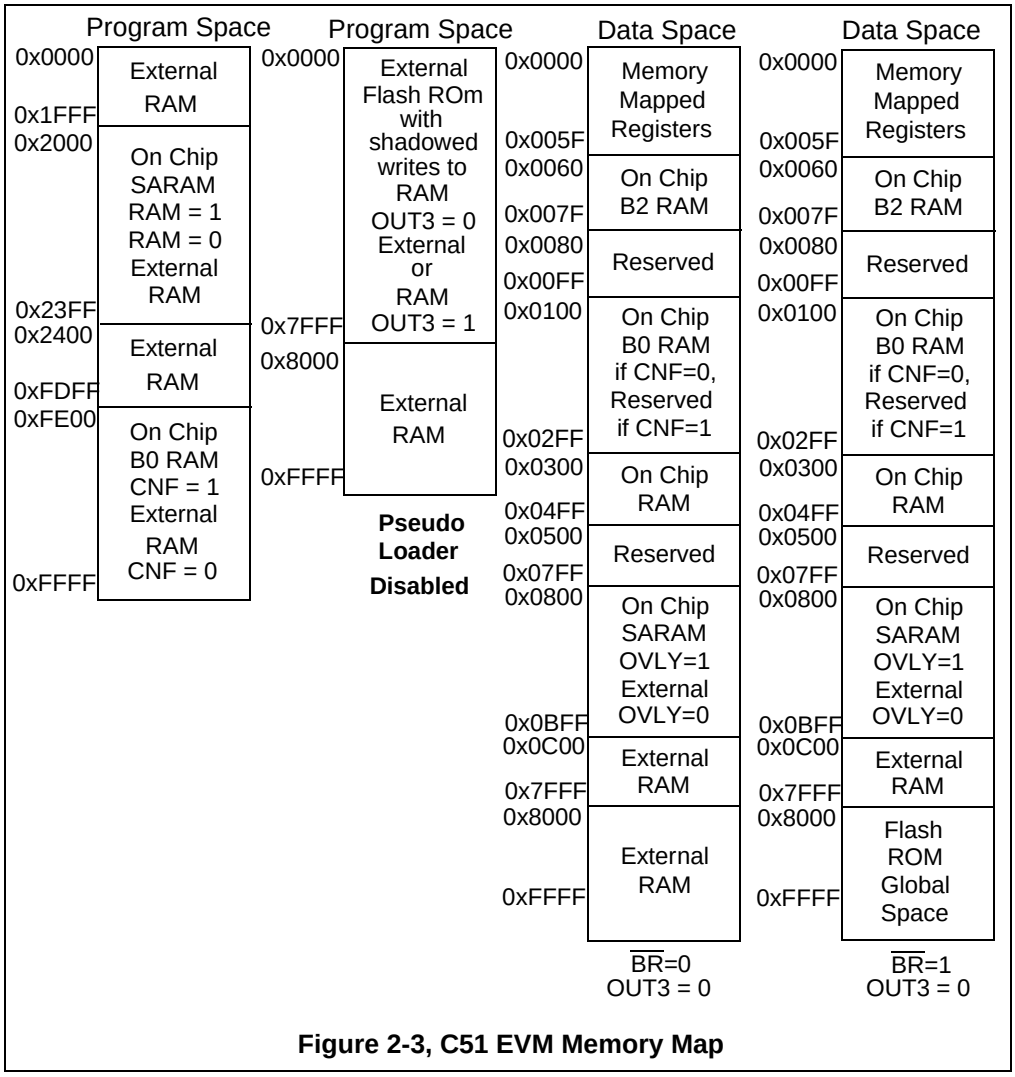


Figure 2-3, C51 EVM Memory Map

The I/O space map for the EVM is shown below:

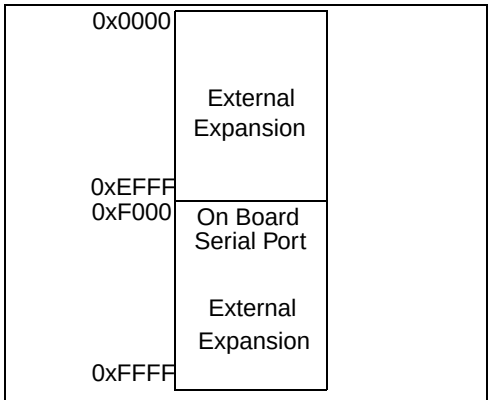


Figure 2-4, C5X EVM I/O Space Map

The C5X EVM can be configured in a variety of ways. The following is a brief outline of configuration for both the C50 and C51.

NOTE

All references to OUT1, OUT2, and OUT3 refer to UART control registers as outlined in Table 4. The pin states are inverted.

The standard as shipped configuration, for the C50 and C51 is an all RAM system which is controlled via jumper JP12. When JP12 is in the 1-2 position and JP11 (which controls the MP/MC- pin) is in the 1-2 position the entire data space and program space are RAM based. Flash ROM is mapped in global data space from 0x8000 to 0xFFFF, but can be deactivated by writing a 1 to the OUT3 bit in the UART's MCR register.

When the user desires to use the EVM in a stand-alone mode either the C50 bootloader or the EVM's pseudo boot loader must be used to allow applications stored in flash to be copied into RAM and executed.

To use the pseudo boot loader jumper JP12 is placed in the 2-3 position with the JP11 jumper in the 1-2 position. In this mode the flash rom is readable in program space 0x0000 to 0x7FFF and read-writable in global data space 0x8000 to 0xFFFF. Writes to 0x0000 to 0x7FFF in program space access external RAM thus the flash rom is "shadowed" by ram allowing the user application to copy itself to ram and begin execution. The primary reason to copy the program to ram is to allow DSP to operate at 0 wait states. After the code is copied into RAM the OUT3 bit is set to 1 disabling the FLASH ROM.

If EVM is populated with a C50 or BC51device the user can use either the pseudo boot loader as previously discussed or the C50's internal boot loader. The EVM supports parallel prom boot mode via the C50's internal boot loader. In this configuration JP11 is in the2-3 position enabling the boot loader, and JP12 is in the 1-2 position enabling the flash rom in global address space. The C50 boot loader will access location 0xFFFF in global data space to identify a key for boot loading. The keys that are applicable for the EVM is shown in the table below.

Table 1: Boot Load Keys

Address	D15 D8	D7 D0	Mode
0xFFFF	xxxx xxxx	SRC | 01	8 bit parallel EPROM
0xFFFF	xxxx xxxx	SRC | 10	16 bit parallel EPROM

The SRC address is the 6 Most Significant Bits (MSBs) of the flash ROM's start address where the boot loadable data is located. In the case of the C5X this typically would be location 0x8000 so the SRC would be 100000b.

The data stored at the SRC field needs to be in one of the following formats shown in Table 2 and Table 3.

Table 2: 16 Bit SRC Field Definitions

Address	Field Definition
0x8000	Destination Address
0x8001	Length
0x8002	Code word #1
.	etc.

Destination is the destination address of where the code will be written, typically 0x0000. Length is the number of 16 bit words to be transferred -1, not including the 2 header words. After the C50 has transferred the data, execution is started at the destination address.

The 8 bit boot mode is similar except that only the lower 8 bits are used and the first location is the MSB. This is shown in the table below:

Table 3: 8 Bit SRC Field Definitions

Address	Field Definition D7 D0
0x8000	Destination Address, high byte
0x8001	Destination Address, low byte
0x8002	Length, high byte
0x8003	Length, low byte
0x8004	Code word 1, high byte
0x8005	Code word 1, low byte

2.2.1 Memory Mapping

Memory mapping is controlled by the jumper JP12 and software output pin OUT3 from the TL16C550 UART as described in the previous section. The table below summarizes the mapping.

Table 4: Memory Map Control Bits

JP12	OUT3(DTR)	Description
1-2	0	Flash Mapped in Global Data Space 0x8000-0xFFFF
1-2	1	Flash Disabled
2-3	0	Flash Mapped in Global Data Space 0x8000-0xFFFF and shadowed in Program Space 0x0000-0x7FFF
2-3	1	Flash Disabled

External memory decode is done via U10 a GAL16V8. The generic array device selects the RAM, FLASH ROM, on board peripherals, or off board peripherals. The equations for the GAL are included in Appendix A. Figure 2-4 shows a zero wait state program space memory read followed by a data space memory write.

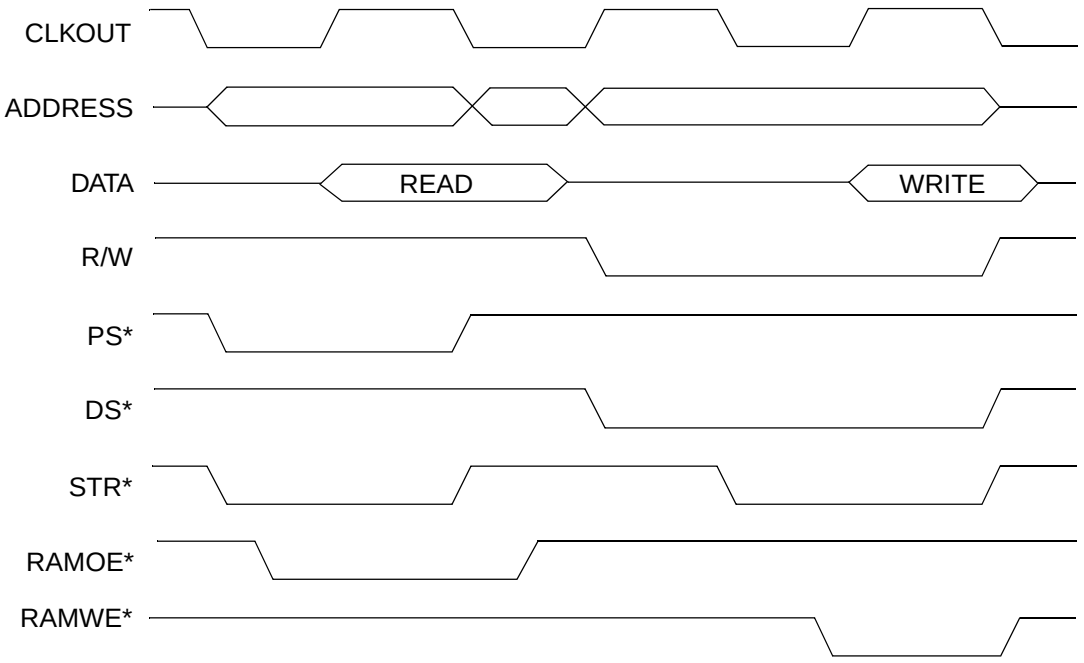


Figure 2-5, Zero Wait State Memory Timing

The external Flash ROM is mapped into the global data space or program space. Note that this memory requires multiple wait states. The main purpose of this memory is to allow for the boot loading of programs from either the C5X's internal boot loader or the pseudo boot loader created in external flash. For more information on the boot loader please refer to the Texas Instruments TMS320C5X Users Guide.

2.3 Expansion Bus

The TMS320C5X EVM has 4 expansion connectors. Each of these carry a specific type of signals. These connectors are used for hardware expansion or customization to meet the application's unique requirements.The four connectors are:

Table 5: Expansion Connectors

Connector	Function
P1	I/O
P2	Analog
P3	Address/Data
P4	Control

I/O accesses from 0x0000 to 0xEFFF are mapped onto the I/O connector. The address data and control lines are not buffered onto these busses. The expansion I/O busses are meant to execute with at least 3 wait states in the IOWSR register to accommodate the onboard UART. However the ready signal can be asserted if a longer access time is required. The next 4 tables describe these connectors.

2.3.1 Expansion I/O Connector, P1

The definition of P1, which has the I/O signals is shown below.

Table 6: P1 I/O

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	TOUT	4	Reserved
5	TDR	6	Reserved
7	TDX	8	Reserved
9	TFSR	10	Reserved
11	TCLKR	12	Reserved
13	TCLKX	14	OUT2
15	3	16	Reserved
17	GND	18	GND
19	XF	20	BIO
21	Resreved	22	Reserved
23	OUT1(UART)	24	OUT3(UART)
25	OUT2(UART)	26	Reserved
27	Reserved	28	Reserved
29	IN1(UART)	30	IN3(UART)
31	IN2(UART)	32	Reserved
33	GND	34	GND

2.3.2 Expansion Analog Connector, P2

The definition of P2, which has the analog signals is shown below.

Table 7: P2 Analog

Pin #	Signal	Pin #	Signal
1	VCCA, +5V Analog	2	VCCA, +5V Analog
3	ADCIN 0 (AD55)	4	Reserved
5	Reserved	6	Reserved
7	Reserved	8	Reserved
9	Reserved	10	Reserved
11	FLAG 0 (AD55)	12	FLAG 1 (AD55)
13	Reserved	14	Reserved
15	Reserved	16	Reserved
17	Reserved	18	Reserved
19	Reserved	20	Reserved
21	Reserved	22	-5V
23	AGND	24	AGND
25	DACOUT 0 (AD55)	26	Reserved
27	Reserved	28	Reserved
29	Reserved	30	Reserved
31	Reserved	32	Reserved
33	AGND	34	AGND

2.3.3 Expansion Address and Data Connector, P3

The definition of P3, which has the address and data signals is shown below.

Table 8: P3 Address/Data

Pin #	Signal	Pin #	Signal
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	GND
19	D0	20	D1
21	D2	22	D3
23	D4	24	D5
25	D6	26	D7
27	D8	28	D9
29	D10	30	D11
31	D12	32	D13
33	D14	34	D15

2.3.4 Expansion Control Connector, P4

The definition of P4, which has the control signals is shown below.

Table 9: P4 Control

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	PS-	4	DS-
5	IS-	6	BR-
7	WE-	8	RD-
9	STRB-	10	R/W
11	READY	12	Reserved
13	RS-	14	TRGRESET-
15	NMI-	16	INT2-
17	GND	18	GND
19	INT3-	20	INT4-
21	DR	22	Reserved
23	DX	24	Reserved
25	FSR	26	Reserved
27	FSX	28	Reserved
29	CLKXR	30	Reserved
31	Reserved	32	CLKOUT
33	GND	34	GND

2.4 Analog Interface

The C5X synchronous serial port can be used to access either the onboard TLC320AD55 sigma delta codec or be jumpered to the expansion connector. Jumper JP4 (1-2) is used to interconnect the serial port to the AD55. If the serial port is to be used from the expansion connector the plug should be in the 2-3 position.

.

Table 10: AIC Signal source

JP4 Position	Signal Source
1-2	TLC320AD55
2-3	Expansion Connector P4

Programming information for the TLC320AD55 is contained in appendix D.

2.4.1 Analog Input, J2

The analog input is driven from either RCA Jack J2 or expansion connector P2. The analog input can be either AC or DC coupled. Jumper JP1 determines if the input is AC or DC coupled.

Table 11: J2 Coupling

JP1 Position	Input Coupling
1-2	DC Coupled
2-3	AC Coupled

2.4.2 Analog Output, J3

The analog output is driven to RCA Jack J3 and expansion connector P2.

2.5 JTAG Interface, P7

The TMS320C5X Evaluation Module is supplied with a 14 pin header interface. This interface is labeled P7 and is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown in the figure below:

TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD (+5V)	5	6	**no pin (key)**	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 2-6, JTAG Interface Pinout

2.6 On Board Serial Interface

The EVM320C5X has a TL16C550 UART (U3) which provides a serial interface. This UART is mapped into I/O space at locations 0xF000 to 0xF008. This device allows users to use this resource for data logging, code debugging and other applications.

The programming of the TL16C550 UART is described in appendix C.

This UART is brought out to connector P5 on the EVM320C5X. Connector P5 is a DB9 female connector. The pin positions for the P5 connector as viewed from the edge of the EVM320C5X.

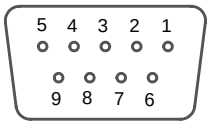


Figure 2-7, P5 Connector

The pin numbers and their corresponding signals are shown in the table below:

Table 12: P5 RS232 Pinout

Pin #	PC (female)	SD EVM
2	Rx, input	Tx, output
3	Tx, output	Rx, input
4	DTR, output	Reset/CTS, input*
5	GND	GND
8	CTS, input	RTS, output

* Jumper JP3 can also be used to configure pin 4 to pin 7 on P5. This allows for normal handshaking. The jumper setting are shown in to table below:

Table 13: JP3 Settings

JP3 Position	CTS Routing
1-2	P5 pin 4 used on CTS input
2-3	P5 pin 7 used on CTS input

Connector P5 pin 4 can be jumpered via JP9 to generate different interrupt levels. The type of interrupt is shown in the table below:

Table 14: Onboard UART Interrupt Selection

JP9 Position	Interrupt Level
1-2	NMI
2-3	INT1

2.7 EVM320C5X Jumpers

The EVM320C5X has 12 jumpers which determine how features on the EVM are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 15: EVM320C5X Jumpers

Jumper #	Size	Function
JP1	1 x 3	J2 Input Coupling
JP2	1 x 3	UART Reset/CTS
JP3	1 x 3	P5 pin 4 Routing
JP4	1 x 3	Synchronous Port Routing
JP5	1 x 3	AD55 Reset Option
JP6	1 x 3	CLKIN Source Select
JP7	1 x 3	CLKIN Source Select
JP8	1 x 3	Ready Option
JP9	1 x 3	Onboard UART Interrupt Select
JP10	1 x 3	CLKIN Source Select
JP11	1 x 3	C50 Bootloader Enable
JP12	1 x 3	Pseudo Boot Loader Enable

Each jumper on the EVM320C5X is a 1 x 3 jumper. Each 1 x 3 jumper **must** have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a ‘1’ on the board’s silkscreen. A top view of this type of jumper is shown below:

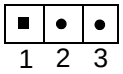


Figure 2-8, Jumper Layout

WARNING !
Unless noted otherwise all jumpers must be installed in either the 1-2 or 2-3 position

2.7.1 J2 Input Coupling Select Jumper, JP1

Jumper JP1 is used to select the coupling for the analog input. If position 1-2 is selected the coupling is DC. The 2-3 selection will provide AC coupling.

Table 16: J2 Coupling

JP1 Position	Input Coupling
1-2	DC Coupled
2-3	AC Coupled

2.7.2 UART Reset Jumper, JP2

Jumper JP2 is used to select either a system reset from the P5, pin 4 DTR line or to connect the DTR line to the UART's CTS pin. When position 1-2 is selected the DTR activates the reset. The 2-3 position connects DTR to CTS. The table below shows the positions and their functions:

Table 17: UART Reset

JP2 Position	Function
1-2	DTR activates Reset
2-3	Connects DTR to CTS*

* See jumper JP15 for choice of pin 4 or pin 7 to CTS on the onboard UART.

2.7.3 On Board UART CTS Routing Jumper, JP3

Jumper JP3 is used to configure the source of the CTS signal on the onboard UART. When position 1-2 is used the pin 4 on P5 is used as the CTS input. If position 2-3 is chosen pin 7 on P5 is used as the CTS input.

Table 18: Onboard UART CTS Routing

JP3 Position	CTS Routing
1-2	P5 pin 4 used on CTS input
2-3	P5 pin 7 used on CTS input

2.7.4 Synchronous Serial Port Routing Jumper, JP4

The JP4 jumper is used to select the source of data for the synchronous serial port on the C5X. By selecting position 1-2 the synchronous serial port is connected to TLC320AD55 AIC. Position 2-3 connects the serial port to the expansion connector P4.

Table 19: Synchronous Serial Port Routing

JP4 Position	Signal Source
1-2	TLC320AD55
2-3	Expansion Connector P4

2.7.5 AD55 Reset Jumper, JP5

The AD55 Codec can be reset either by the system reset or the I/O0 pin on the C5X. Position 1-2 allow the AD55 to be reset by the system reset. In position 2-3 the AD55 is reset from the I/O0 pin on the DSP. The table below shows the positions and their functions:

Table 20: AD55 Reset

JP5 Position	Function
1-2	System reset activates AD55 reset
2-3	C5X I/O0 pin activates AD55 reset

2.7.6 CLKIN Source Select Jumper, JP6,JP7, JP10

The C5X EVM is equipped with a 40 Megahertz oscillator. Jumpers JP6, JP7, and JP10 determine if the output clkout frequency is 20 Megahertz (divide by 2, 20 MIPS) or 40 Megahertz (divide by 1, 40 MIPS). Note there are only two valid configurations.

Table 21: CLKIN Source Select

JP6 Position	JP7 Position	JP10 Position	Output Clock
CLKIN	CLKIN2	CLKMDI	C5X Pin
1-2	1-2	1-2	40 Mhz CLKOUT
2-3	2-3	2-3	20 Mhz CLKOUT

2.7.7 READY Routing Jumper, JP8

READY to the C5X device from the GAL U11 can be deactivated if necessary. Of course this prevents use of the onboard UART if the wait state generator is set to less than 7 wait states. In normal mode (position 1-2) external READY from the I/O connector is routed through GAL U11. When JP8 is in the 2-3 position the READY signal is routed directly from the expansion connector to the C5X device. The table below shows the positions and their functions:

Table 22: READY Routing

JP8 Position	Function
1-2	READY from GAL U11
2-3	READY directly from I/O expansion connector

2.7.8 Onboard UART Interrupt Select Jumper, JP9

The jumper JP9 is used to select which interrupt the onboard UART will use. Position 1-2 will cause an NMI interrupt. Position 2-3 will cause INT1.

Table 23: Onboard UART Interrupt Selection

JP9 Position	Signal
1-2	NMI
2-3	INT1

This option is used to allow a debug monitor to be placed in ROM or for the serial port to be used with application software which requires interrupt masking.

2.7.9 C50 Bootloader Enable Jumper, JP11

Jumper JP11 is used to enable or disable the on chip bootloader on the TMS320C5X. The table below describes the two positions:

Table 24: Bootload Enable/Disable

JP11 Position	Function
1-2	Boot enabled on C50
2-3	Boot disabled on C50

2.7.10 Pseudo Boot Loader Enable Jumper, JP12

Jumper JP12 is used to indicate whether the pseudo boot loader is enabled on the EVM. This input is used by the memory decode logic. When the pseudo boot loader is enabled external flash is mapped in at 0x0000-0x7FFF in program space. When the pseudo loader is disabled the entire program space is RAM.

Table 25: Jumper JP12

JP12 Position	Device Selected
1-2	Pseudo Boot Loader Disabled
2-3	Pseudo Boot Loader Enabled

2.8 LEDs

The TMS320C230 EVM has two light emitting diodes. DS1 indicates the presence of +5 volts and is normally ‘on’ when power is applied to the EVM320C5X board. DS2 is under software control. It is tied to the XF signal on the DSP. These are shown in the table below:

Table 26: LEDs

LED #	Color	Controlling Signal	On Signal State
DS1	Green	+5 Volts	1
DS2	Red	XF	1

2.9 Resets

There are multiple resets for the TMS320C50 EVM. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320C5X.

External sources such as the push button(SW1), Host reset pin 4 on P4 UART interface, and pin p13 on the Control connector P4 can generate a reset condition.

Appendix A

TMS320C5X EVM PAL Equations

This appendix lists the two PAL logic equations that are used on the TMS320C5X Evaluation Module (EVM).

Topic **Page**

A.1	**Memory Decode Equations**	**A-2**
A.2	**I/O Control Equations**	**A-4**

A.1 Memory Decode PAL Equations

The following PAL equations are used for the memory decode logic

```
/*
**  503403.tdl
**  Drawing Number: 503403
**  Company: Spectrum Digital Inc
**  Engineer: Ron Peterson
**  'G16V8' is defined (usually with the /D option).
*/

503403 (in      is,         /* io space         */
                ds,         /* data space       */
                ps,         /* program space    */
                rw,         /* read write       */
                stb,        /* strobe           */
                we,         /* write strobe     */
                rd,         /* read strobe      */
                br,         /* Global Data Space    */
                a15,        /* address          */
                out3,       /* expanded rom enable  */
                uart,       /* UART CYCLE INPUT     */
                opt0;       /* Option 0         */
        out     !eprom,     /* ROM  cycle       */
                !ramwe,     /* RAM WRITE CYCLE      */
                !ramoe,     /* RAM READ CYCLE       */
                !intern;    /* internal long cycle  */
        )
{


intern.oe  = 1;
ramoe.oe   = 1;
ramwe.oe   = 1;
eprom.oe   = 1;
```

```
  /* equations */


ramoe =   ( !ps & rw & !stb & out3 & a15& opt0 )        /* program space 0x8000-0xffff no out    */
            | ( !ps & rw & !stb & !out3 & opt0 )        /* program space 0x0000-0xffff with out  */
            | ( !ps & rw & !stb & !opt0 )          /* program space 0x0000-0xffff psuedo disabled*/
            | ( !ds & rw & !stb & br )                  /* data space    0x0000-0xffff no br     */
            | ( !ds & rw & !stb & !a15 & !br );          /* data space    0x0000-0x7fff with br   */

ramwe =  ( !ps & !rw & !stb )                           /* program space 0x0000-0xffff           */
            | ( !ds & !rw & !stb & br )                  /* data space    0x0000-0xffff no br     */
            | ( !ds & !rw & !stb & !a15 & !br );          /* data space    0x0000-0x7fff with br   */


/* FLASH ROM (Bootload)  external DATA SPACE 0x8000 - 0xffff ie br low */

eprom  =  (  a15 & !br & !we & !ds & out3 )     /* Write Global Space 0x8000 with no out3        */
           | (  a15 & !br & !rd & !ds & out3 )     /* Read Global space 0x8000 with no out3         */
           | ( !a15 & !rd & !ps & out3 & opt0 ); /* Program space 0x0000-0x7fff no out3 psuedo en*/



/* 0xF000 in io space  for UART chip */

intern =    (  a15 & !br & !we & !ds  & out3 )    /* Write to flash in global data space      */
            | ( !a15 &   !rd & !ps & out3& opt0)  /* Flash in program space 0x0000-0x7fff */
            | (  a15 & !br & !rd & !ds & out3 )    /* Read from flash in global data space   */
            | (  !uart & !rd      )               /* UART Read   */
            | (  !uart & !we      );              /* UART Write   */



putpart("g16v8", "503403A",
          is,   ps,  ds, rw, stb, we, rd, br, out3, GND,
          a15,  eprom,  _, ramwe,  ramoe, opt0,  _, uart, intern, VCC);


}
```

A.2 I/O Control PAL Equations

The following PAL equations are used for the I/O control logic

```
/*
**  503404.tdl
**  Drawing Number: 503404
**  Company: Spectrum Digital Inc
**  Engineer: Ron Peterson
**  'G16V8' is defined (usually with the /D option).
*/
503404 (in      clk,          /* clock                */
                is,           /* io select            */
                rw,           /* read write           */
                stb,          /* strobe               */
                a15,          /* address              */
                a14,          /* address              */
                a13,          /* address              */
                a12,          /* address              */
                trdy,         /* target ready         */
                !reset,       /* reset                */
                oe;
        out     ready;        /* ready out            */
                io reg state0, /* io start machine 0  */
                state1,       /* io state machine 1   */
                state2;       /* io state machine 2   */
         io     uartwe,       /* io write strobe      */
                uartrd,       /* io read strobe       */
                uartcs;       /* uart chip select     */
        )
{
group cntl_state[state2,state1,state0];

                /* SSS       */
                /* TTT       */
                /* 210       */
                /*           */

#define IDLE    0b111       /*  X  */

#define STATE1  0b011       /* 25  */
#define STATE2  0b001       /* 50  */
#define STATE3  0b000       /* 75  */
#define STATE4  0b010       /* 75  */
#define COMPLETE  0b110     /*     */

#define UNDEF0  0b100       /*     */
#define UNDEF1  0b101       /*     */
```

```
#define UART ( !is & !stb & a15 & a14 & a13 & a12 )


cntl_state.oe  = !oe;          /* hook up output enables      */
cntl_state.ck  = clk;          /* hook up clocks              */


/* state machines */

switch( cntl_state[] )
  {
       case IDLE:
            if ( reset)
                cntl_state = IDLE;
            else
            {
                 if( UART )
                   cntl_state = STATE1;
                 else
                   cntl_state = IDLE;
            }

            break;


       case STATE1:

            if ( reset )
               cntl_state = IDLE;
            else
            {
                cntl_state = STATE2;
            }
            break;


       case STATE2:

            if ( reset )
               cntl_state = IDLE;
            else
            {
               cntl_state = STATE3;
            }
            break;
```

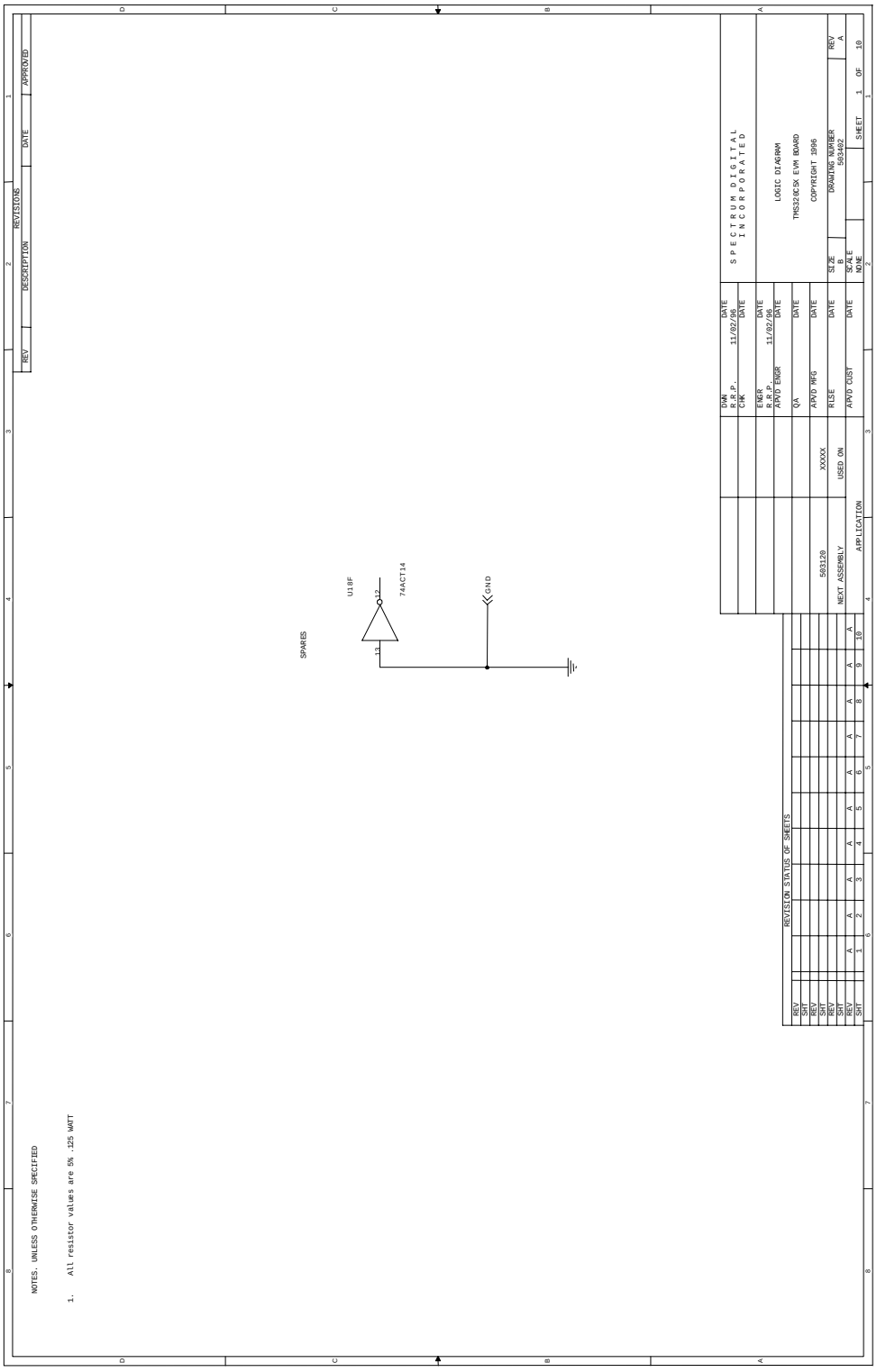
```
        case STATE3:

             if ( reset )
                cntl_state = IDLE;
             else
             {
                cntl_state = STATE4;
             }
             break;

        case STATE4:

             if ( reset )
             {
                cntl_state = IDLE;
             }
             else
             {
                cntl_state = COMPLETE;
             }
             break;

        case COMPLETE:
             if( reset )
             {
               cntl_state = IDLE;
             }
             else
             {
              if( UART )
                 cntl_state = COMPLETE;
              else
                 cntl_state = IDLE;
             }
             break;

        case UNDEF0:
             cntl_state = IDLE;
             break;
        case UNDEF1:
              cntl_state = IDLE;
              break;

        default:
             cntl_state = IDLE;
             break;
   }
```

```
/* equations */


!uartcs = UART;

!ready =    ((cntl_state == STATE2)  &UART )
              | ((cntl_state == STATE3) &  UART )
              | ((cntl_state == STATE4) &  UART )
              | (!trdy );

!uartwe = ((cntl_state == STATE2) & !rw & UART )
              | ((cntl_state == STATE3) & !rw & UART )
              | ((cntl_state == STATE4) & !rw & UART );

!uartrd = (( cntl_state == STATE2) & rw & UART )
              | (( cntl_state == STATE3) & rw & UART )
              | (( cntl_state == STATE4) & rw & UART )
              | ( !uartrd & UART /*rw & !stb*/ );


putpart("g16v8r", "503404A",
          clk, is, rw, stb, a15, a14, a13, a12, trdy, GND,
          oe, uartwe, uartcs, state0, uartrd, state1, state2, reset, ready, VCC);


}
```

Appendix B

TMS320C5X EVM Schematics

This appendix contains the schematics for the TMS320C5X EVM. The schematics were drawn on ORCAD.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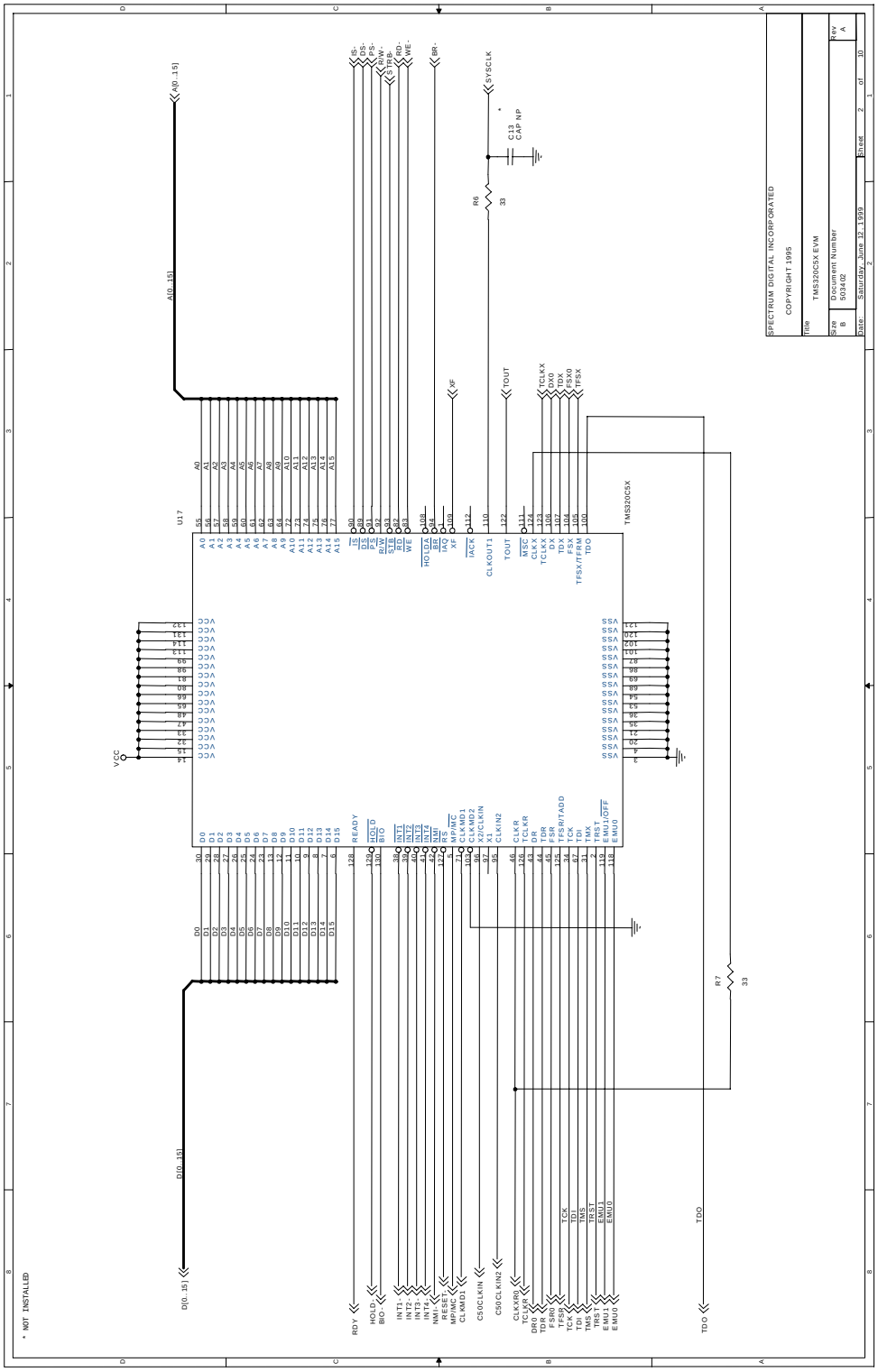
503102
SIZE
B
SCALE
NONE
SHEET 1 OF 10
REV A
DWN R.R.P. 11/02/96
CHK
ENGR R.R.P. 11/02/96
ANVD ENGR
QA
ANVD MFG
RLSE
ANVD CUST
503129
XXXXX
USED ON
NEXT ASSEMBLY
APPLICATION
REVISION STATUS OF SHEETS
SPARES
U18F
74ACT14
GND
NOTES. UNLESS OTHERWISE SPECIFIED
1. All resistor values are 5% .125 WATT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Sheet
2
of
10
U17
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A[0..19]
D[0..15]
VCC
R6
33
C13
CAP NP
R7
33
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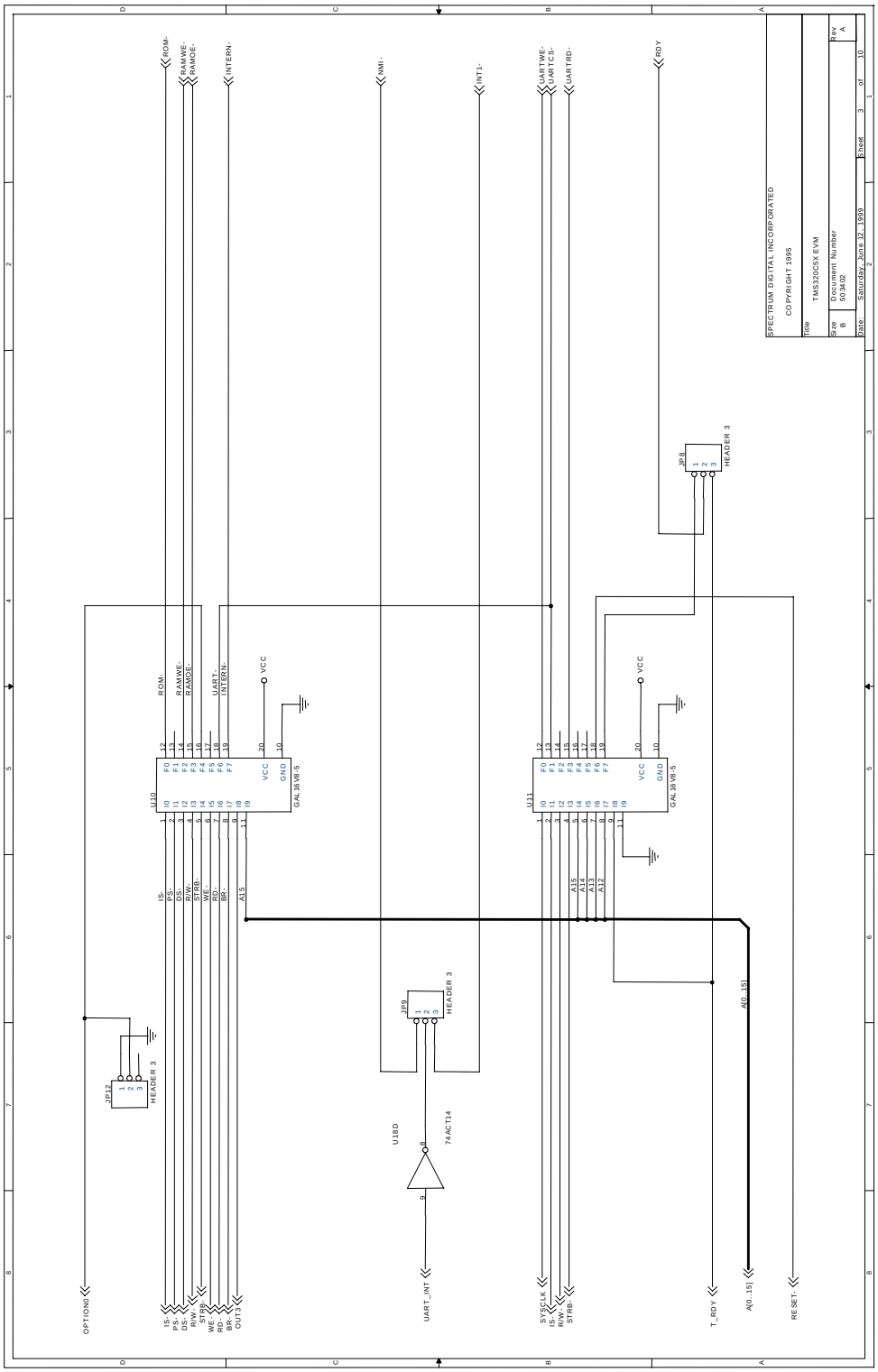
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RAMWE-
RAMDE-
INTERN-
NMI-
INT1-
UARTWE-
UARTCS-
UARTRD-
RDY
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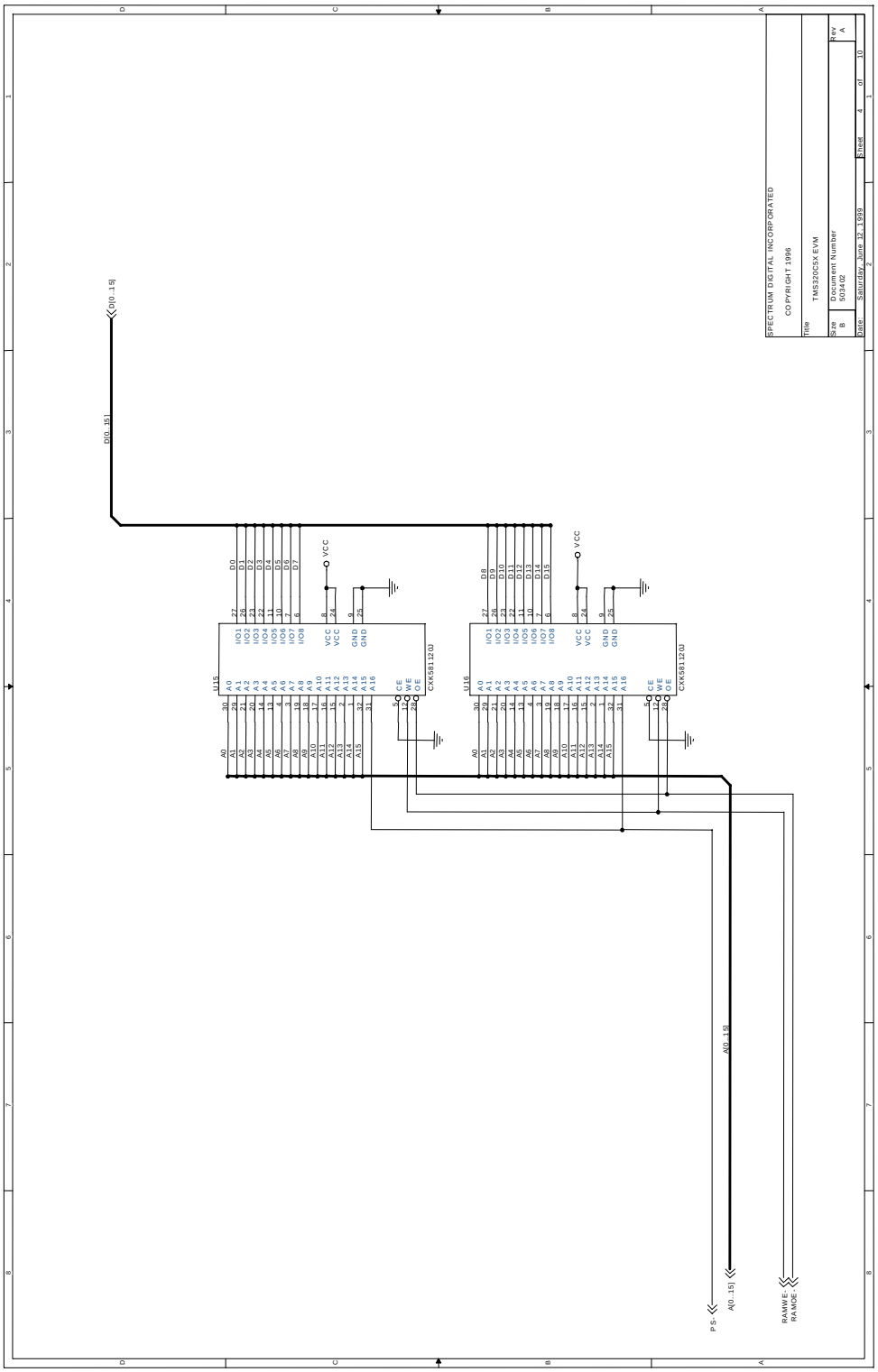
10
U10
GAL16V8-5
U11
GAL16V8-5
VCC
GND
JP8
HEADER 3
JP12
HEADER 3
JP9
HEADER 3
U18D
74ACT14
OPTION0
IS-
PS-
DS-
R/W-
STRB-
WE-
RD-
BR-
OUT3
UART_INT
SYSCLK
T_RDY
A0..15]
RESET-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Sheet
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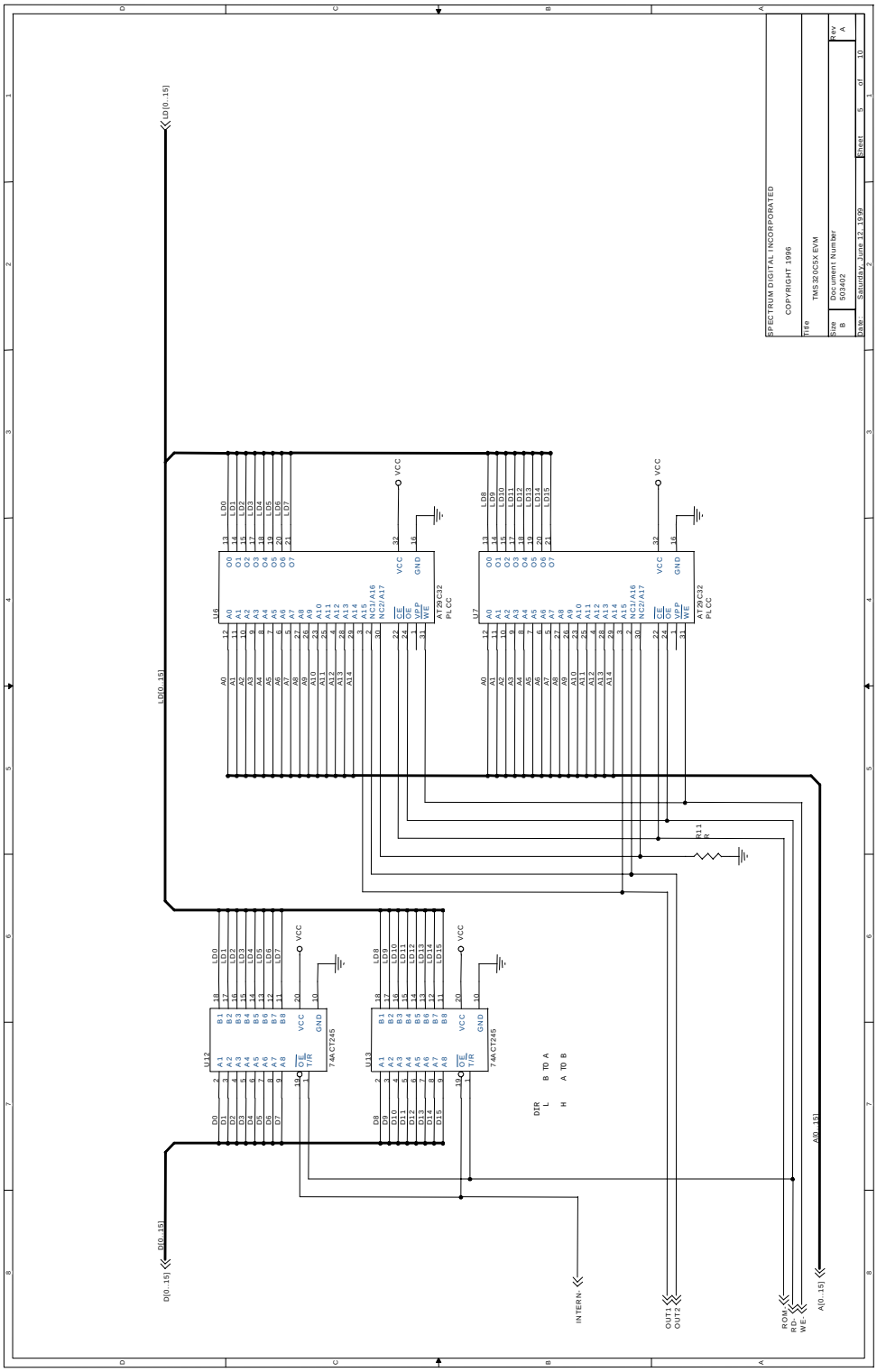
D[0..15]
A[0..15]
U16
U15
CXK581270
VCC
GND
CE
WE
OE
PS-
RAMWE-
RAMOE-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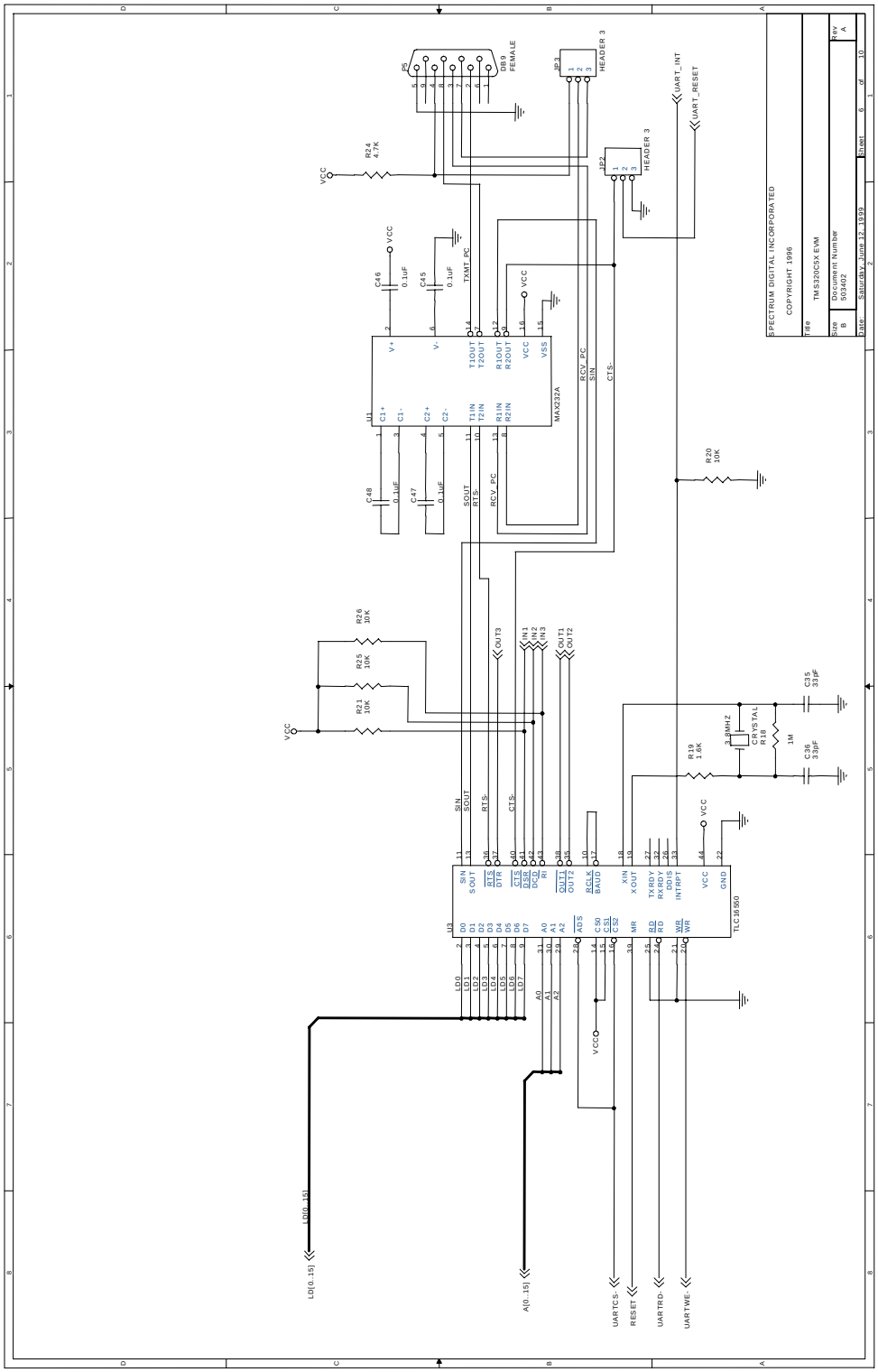
LD[0..15]
A[0..15]
U6
U7
U12
U13
74ACT245
AT29C32
PLCC
VCC
GND
DIR
L B TO A
H A TO B
INTERN-
OUT1
OUT2
R/W-
RD-
WE-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TLC16560
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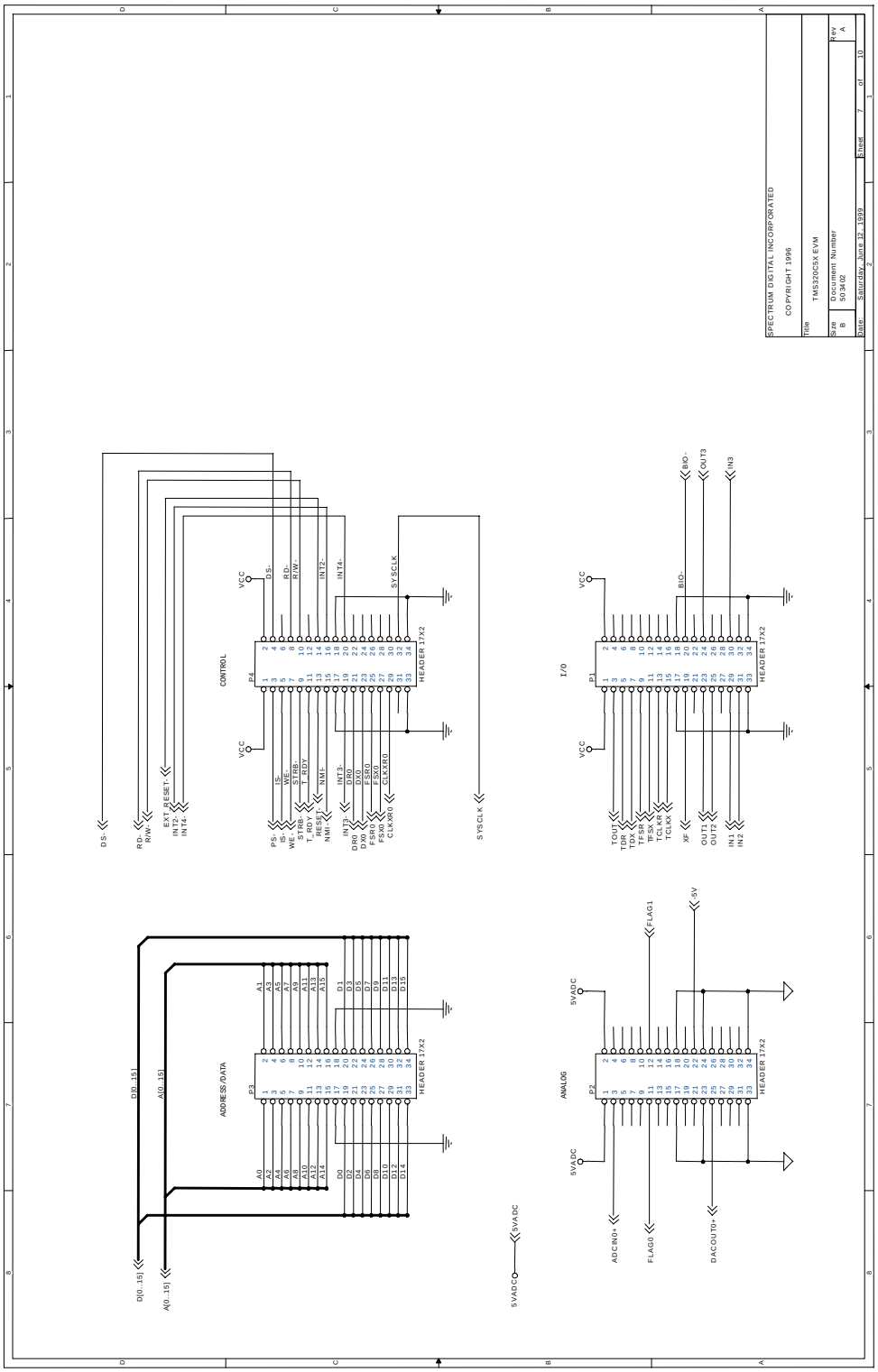
DB9M FEMALE
UART_INT
UART_RESET
XTAL
3.6864Z
VCC
LD[0..15]
A[0..15]
UARTCS-
RESET
UARTRD-
UARTWE-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Sheet
7
of
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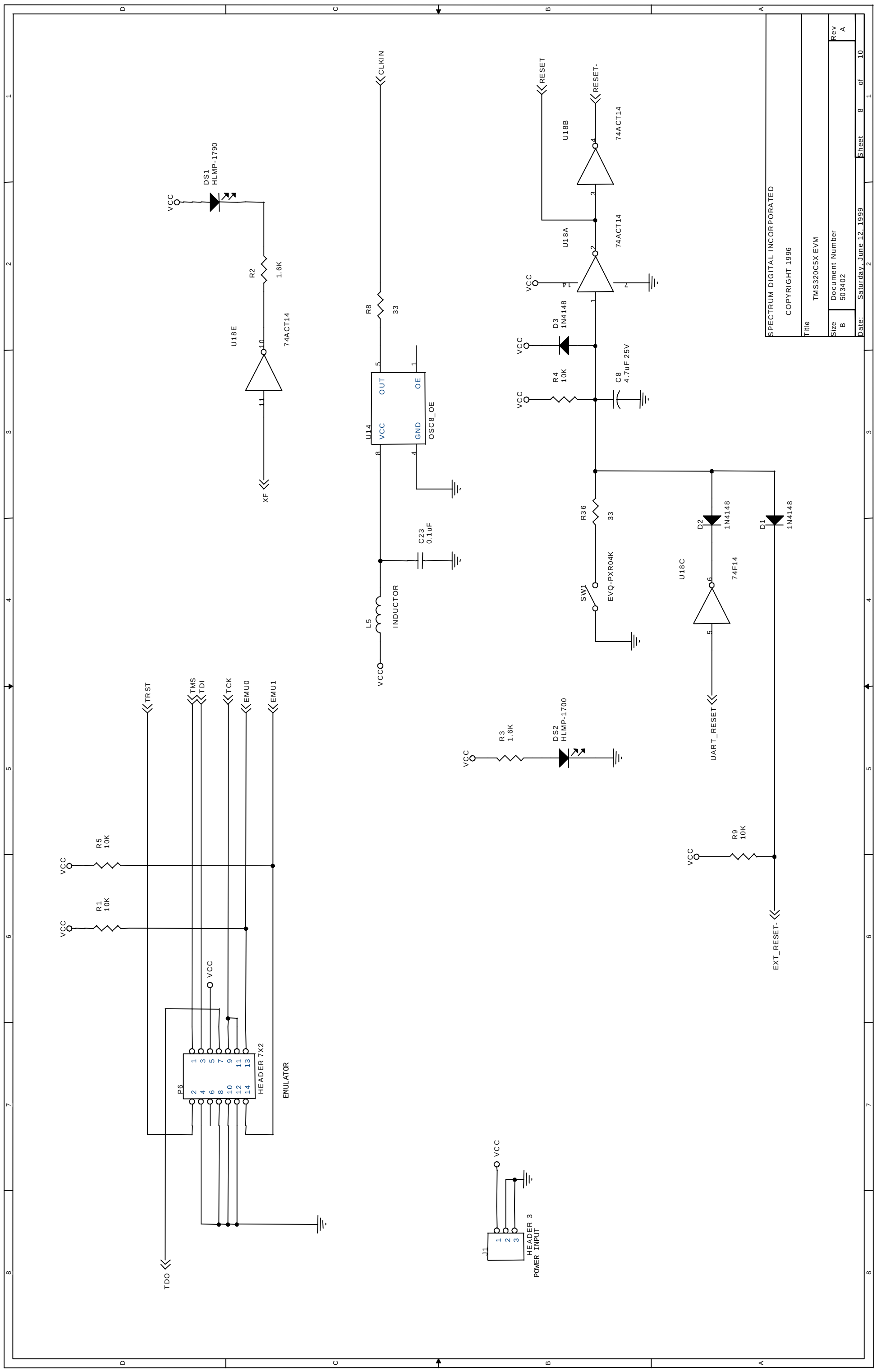
CONTROL
I/O
ANALOG
ADDRESS/DATA
HEADER 17X2
VCC
5VADC
SYSCLK
D[0..15]
A[0..15]
DS-
RD-
R/W-
EXT RESET
INT2-
INT4-
BIO-
OUT3
IN3
FLAG1
3V
FLAG0
ADCIN0+
DACOUT0+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Date
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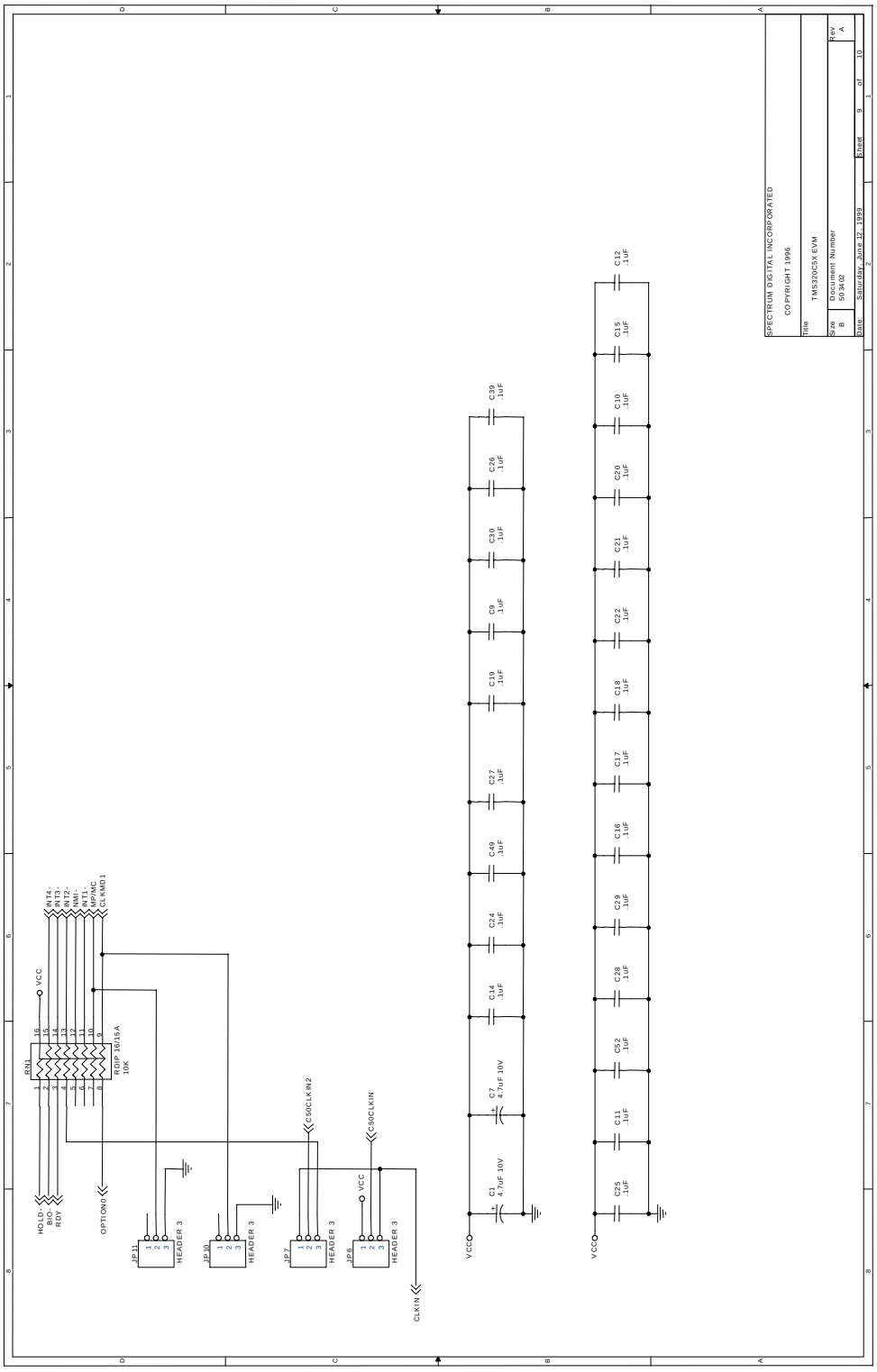
Sheet
8
of
10
CLKIN
RESET
RESET-
U18B
74ACT14
U18A
74ACT14
DS1
HLMP-1790
VCC
R2
1.6K
U18E
74ACT14
XF
R8
33
U14
OSC8_OE
OUT
OE
VCC
GND
C23
0.1uF
L5
INDUCTOR
D3
1N4148
R4
10K
C8
4.7uF 25V
R36
33
SW1
EVQ-PXR04K
D2
1N4148
D1
1N4148
U18C
74F14
UART_RESET
R3
1.6K
DS2
HLMP-1700
R9
10K
EXT_RESET-
TRST
TMS
TDI
TCK
EMU0
EMU1
R5
10K
R1
10K
P6
HEADER 7X2
EMULATOR
TDO
J1
HEADER 3
POWER INPUT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Sheet
9
of
10
VCC
RN1
RDIP 16J15A
10K
RN4-
RN3-
RN2-
NMI-
RN1-
XRS-
CLKMD1
HOLD-
BIO-
RDY
OPTION0
JP11
JP10
JP7
JP6
HEADER 3
C50CLKIN2
C50CLKIN
CLKIN
C1
4.7uF 10V
C7
4.7uF 10V
C14
.1uF
C24
.1uF
C49
.1uF
C27
.1uF
C19
.1uF
C9
.1uF
C30
.1uF
C26
.1uF
C39
.1uF
C25
.1uF
C11
.1uF
C52
.1uF
C28
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C29
.1uF
C16
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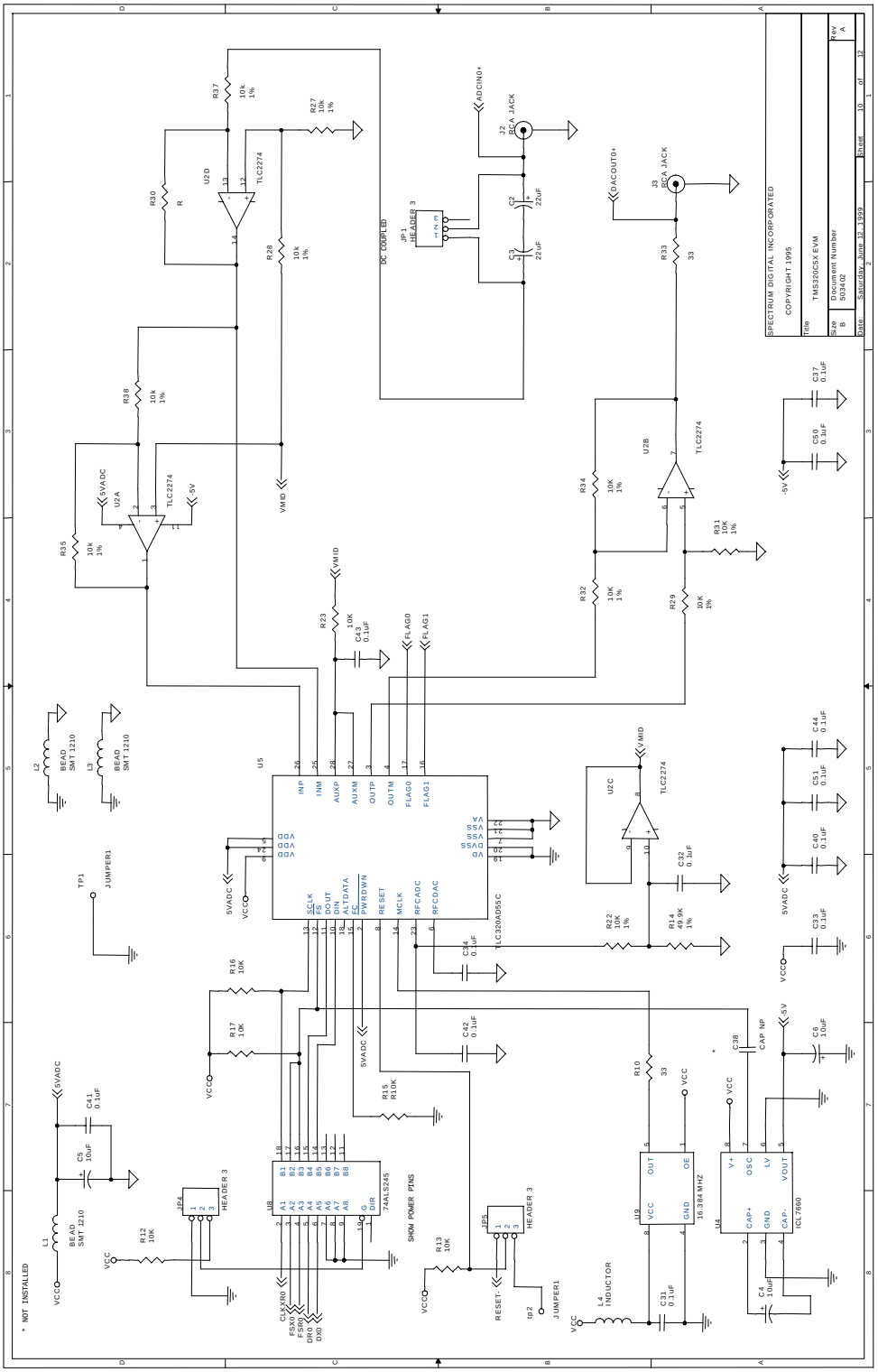
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10
of
12
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DC COUPLED
SHOW POWER PINS
ADCIN0+
DACOUT0+
VMID
5VADC
-5V
VCC
RESET-
CLKX0
FSX0
FSR0
DR0
DX0
TLC2274
TLC320AD55C
74ALS245
16.384 MHZ
ICL7660
JUMPER1
HEADER 3
BEAD SMT 1210
INDUCTOR
CAP NP

Appendix C

TL16C550 Data Sheet

This appendix contains the programming data sheet for the TL16C550 Asynchronous Communications Element (ACE) used on the TMS320C5X Evaluation Module (EVM).

Topic **Page**

C.1	TL16C550 Serial Controller	C-2
C.1.1	Detailed Description	C-2
C.1.2	Line Control Register	C-4
C.1.3	Line Status Register	C-6
C.1.4	FIFO Control Register	C-8
C.1.5	Modem Control Register	C-9
C.1.6	Modem Status Register	C-10
C.1.7	Divisor Latches	C-12
C.1.8	Scratchpad Register	C-13
C.1.9	Interrupt Identification Register	C-13
C.1.10	Interrupt Enable Register	C-15
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C.1 TL16C550 SERIAL CONTROLLER

The EVM320C5X uses a TL16C550 serial controller. The following sections describe the functionality of this device as it is used in the EVM320C5X.

The TL16C550 UART resides at address 0xF000 in the I/O address space on the EVM320C5X.

C.1.1 DETAILED DESCRIPTION

Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR (7) refers to line control register bit 7.

The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered so that read and write operations may be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

The table below shows the I/O address of the various registers in the TL16C550 as they are used on the EVM320C5X. For more detailed use of this part refer to the appropriate data book.

Table 1: SUMMARY OF ACCESSIBLE REGISTERS

I/O ADDRESS RS232	REGISTER MNEMONIC	REGISTER BIT NUMBERS							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0xF000	RBR (read only)	Data	Data	Data	Data	Data	Data	Data	Data
0xF000	THR (write only)	Data	Data	Data	Data	Data	Data	Data	Data
0xF000 t	DLL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF000 t	DLM	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0xF001	IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver line status interrupt	(ETBEI) Enable Transmit-ter hold-ing register empty interrupt	(ERBI) Enable received data available interrupt
0xF002	FCR (write only)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO Enable
0xF002	IIR (read only)	FIFOs Enabled tt	FIFOs Enabled tt	0	0	Int ID Bit (2) tt	Int ID Bit (1) tt	Int ID Bit (0)	0 if Int Pending
0xF003	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity Enable	(STB) Num of stop bits	(WLSB1) Word len select bit 1	(WLSB0) Word len select bit 0
0xF04	MCR	0	0	0	Loop	Enable external int (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data ter-minal ready
0xF005	LSR	Error in RCVR FIFOtt	(TEMT) transmit-ter empty	(THRE) Transmit-ter hold-ing register empty	(BI) Break interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun error	(DR) Data ready
0xF006	MSR	(DCD) Data carrier detect	(RI) Ring Indicator	(DSR) Data set ready	(CTS) Clear to send	(DDCD) Delta data car-rier detect	(TERI) Trailing edge ring indicator	(DDSR) Delta data set ready	(DCTS) Delta clear to send
0xF007	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

t DLAB 1

tt These bits are always 0 when FIFOs are disabled.

C.1.2 LINE CONTROL REGISTER (0xF003)

The format of the data character is controlled by the Line Control Register. The LCR may be read. Its contents are described below and shown in Figure 1.

LCR(0) and LCR(1) Word Length Select Bits:

Table 2: WORD LENGTH SELECT

LCR1	LCR0	Data bits
0	0	5 data bits
0	1	6 data bits
1	0	7 data bits
1	1	8 data bits

LCR(2) Stop Bits Select Bit 2:

LCR(2) specifies the number of stop bits in each transmitted character as shown below and in table 21. The receiver always checks for one stop bit.

Table 3: STOP BIT SELECT

LCR2	Stop Bits
0	1 Stop Bit
1	1.5 Stop bits if 5 data bits selected
1	2 Stop bits if 6,7,8 data bits selected

LCR(3) Parity Enable Bit 3:

When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select Bit 4:

When enabled, a logic one selects even parity.

LCR(5) Stick Parity Bit 5:

When parity is enabled (LCR(3) = 1, LCR(5) = 1) causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR(4). This forces parity to a known state and allows the receiver to check the parity bit in a known state.

LCR(6) Break Control Bit 6:

When LCR(6) is set to a logic 1, the serial output (SOUT1/SOUT0) is for forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. If the following sequence is used, no invalid characters will be transmitted because of the break:

Step 1. Load a zero byte in response to the Transmitter Holding Register Empty (THRE) status indication.

Step 2. Set the break in response to the next THRE status indication.

Step 3. Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT=1). Then clear the break when the normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB) bit 7:

Bit 7 must be set high (logic 1) to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR(7) must be input low (logic 0) to access the receiver buffer register, the transmitter holding register or the interrupt enable register.

C.1.3 LINE STATUS REGISTER (0xF005)

The line status register (LSR) is a single register that provides status indications. The line status register shown in table 21 and described below:

LSR(0) Data Ready (DR) Bit 0:

Data Ready is set high when an incoming character has been received and transferred into the receiver buffer register or the FIFO. LSR(O) is reset low by a CPU read of the data in the receiver buffer register or the FIFO.

LSR(1) Overrun Error (OE) bit 1:

Overrun Error indicates that data in the receiver buffer register was not read by the CPU before the next character was transferred into the receiver buffer register overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the line status register. An overrun error will occur in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO but it is overwritten.

LSR(2) Parity Error (PE) bit 2:

Parity Error indicates that the received data character does not have the correct parity as selected by LCR(3) and LCR(4). The PE bit is set high upon detection of a parity error and is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO, LSR(2) resets the error when the character is at the top of the FIFO.

LSR(3) Framing Error (FE) bit 3:

Framing error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR(3) reflects the error when the character is at the top of the FIFO.

LSR(4) Break Interrupt (BI) bit 4:

Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the line status register. In the FIFO mode, this is associated with a particular character in the FIFO. LSR(2) reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR(4) - LSR(1) are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the Interrupt Identification register(IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2) = 1 in the interrupt enable register.

LSR(5) Transmitter Holding Register Empty (THRE) bit 5:

THRE Indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the transmitter holding register into the transmitter shift register. LSR(5) is reset low by the loading of the transmitter holding register by the CPU. LSR(5) is not reset by a CPU read of the LSR. In the FIFO mode when the XMIT FIFO is empty, this bit is set. It is cleared when one byte is written to the XMIT FIFO. When the THRE Interrupt is enabled by IER(1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated In IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT) bit 6:

TEMT is set high when the Transmitter Holding Register(THR) and the Transmitter Shift Register(TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR. In FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set to one.

LSR(7) RCVR FIFO error bit 7:

The LSR(7) bit is always 0 in the TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break interrupt indication. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

NOTE:

The line status register may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

C.1.4 FIFO CONTROL REGISTER (0xF002)

This write only register is at the same location as the IIR. It is used to enable and clear the FIFOs, set the trigger level of the RCVR FIFO, and select the type of DMA signaling.

FCR(0) FIFO Enable

FIFO enables both the XMIT and RCVR FIFOS. All bytes in both FIFOs can be cleared by resetting FCR(0). Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR(0) = 1.

FCR(1) Receiver FIFO Reset

FCR(1) = 1 clears all bytes In the RCVR FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR(2) Transmit FIFO Reset

FCR(2) = 1 clears all bytes In the XMIT FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR(3) DMA Mode Select

FCR(3) = 1 will change the RXRDY and TXRDY pins from mode 0 to mode 1 if FCR(0) = 1.

FCR(4) - FCR(5):

These two bits are reserved for future use.

FCR(6-7) FIFO Receiver Trigger

These two bits are used for setting the trigger level for the RCVR FIFO Interrupt a follows:

Table 4: FIFO Trigger Levels

Bit 7	Bit 6	Receiver Fifo Trigger Level (Bytes)
0	0	1
0	1	4
1	0	8
1	1	14

C.1.5 MODEM CONTROL REGISTER (0xF004)

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Figure 2. MCR can be written and read. The RTS and DTR outputs are directly controlled by their control bits in this register. A high input asserts a low(true) at the output pins. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

MCR(0) Data Terminal Ready

When MCR(0) is set high, the DTR output is forced low. When MCR(0) is reset low, the DTR output is forced high. The DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1) Request to Send

When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the RTS output is forced high. The RTS output of the serial channel may be input into an inverting line driver to obtain the proper polarity input at the modem or data set.

MCR(2) OUT1

When MCR(2) is set high, OUT1 is forced low.

MCR(3) OUT2

When MCR(3) is set high, the OUT2 output is forced low.

MCR(4) Loop

MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, serial output (SOUT) is set to the marking (logic 1) state, and the receiver data input serial input (SIN) is disconnected. The output of the transmitter shift register is looped back into the receiver shift register input. The four modem control inputs (CTS, DSR, DCD, and RI) are disconnected. The modem control outputs (DTR, RTS, OUT1, and OUT2) are internally connected to the four modem control inputs. The modem control outputs pins are forced to their inactive state(high) on the TL16C550. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmission and receive data paths of the selected serial channel. Interrupt control is fully operational. However, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external pins represented by those four bits.

MCR(5) - MCR(7) are permanently set to logic 0.

C.1.6 MODEM STATUS REGISTER (0xF006)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem in inputs changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state and reset low when the CPU reads the MSR.

The modem input lines CTS, DSR, RI and DCD. MSR(4) - MSR(7) are status indications of these lines. A status bit = 1 indicates the input is a low. A status bit = 0 indicates the input is high. If the modem status interrupt in the interrupt enable register is enabled IER(3), an interrupt is generated whenever MSR(0) - MSR(3) is set to a one. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 3.

MSR(0) Delta Clear to Send (DCTS) bit 0:

DCTS displays that the CTS input to the serial channel has changed state since it was last read by the CPU.

MSR(1) Delta Data Set Ready (DDSR) bit 1:

DDSR indicates that the DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI) bit 2:

TERI indicates that the RI input to the serial channel has changed state from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DDCD) bit 3:

DDCD indicates that the DCD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS) bit 4:

CTS is the complement of the CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output(SOUT). If the serial channel is in the loop mode MCR(4) = 1, MSR(4) reflects the value of RTS in the MCR.

MSR(5) Data Set Ready (DSR) bit 5:

DSR is the complement of the DSR input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial channel receiver circuitry, If the channel is in the loop mode MCR(4) = 1, MSR(5) reflects the value of DTR in the MCR.

MSR(6) Ring Indicator (RI) bit 6:

RI is the complement of the RI input. If the channel is in the loop mode MCR(4) = 1, MSR(6) reflects the value of OUT1 in the MCR.

MSR(7) Data Carrier Detect (DCD) bit 7:

Data carrier detect indicates the status of the data carrier detect DCD input. If the channel is in the loop mode MCR(4) = 1, MSR(7) reflects the value of OUT2 in the MCR.

Reading the MSR register clears the delta modem status indications but has no effect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read operation, the status bit is not set until the trailing edge of the read. If a status bit is set during a read operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read instead of being set again. In the loop back mode, when modem status interrupts are enabled, the CTS, DSR, RI and DCD input pins are ignored. However a modem status interrupt may still be generated by writing to MCR3 - MCR0. Applications software should not write to the modem status register.

C.1.7 DIVISOR LATCHES (DLAB=1, 0xF000, 0xF001)

The ACE serial channel contains a programmable baud-rate generator (BRG) that divides the clock (dc, to 8 MHz) by any divisor from 1 to 216-1 (also see BRG description). The output frequency of the baud generator is 16X the data rate (divisor # = clock / (baud rate x 16)) referred to in this document as RCLK. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG uses an oscillator frequency of 1.8432Mhz or 3.6864Mhz. which provides the standard baud rates shown in the table below.

Table 5: BAUD RATES

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16X CLOCKS (1.8432Mhz)	DIVISOR (N) USED TO GENERATE 16X CLOCKS (3.6864Mhz)*
50	2304	4608
75	1536	3072
110	1047	2094
134.5	857	1714
150	768	1536
300	384	768
600	192	384
1200	96	192
1800	64	128
2000	58	116
2400	48	96
3600	32	64
4800	24	48
7200	16	32
9600	12	24
19200	6	12
38400	3	6
56000	2	4
115200	1	2

* Used on EVM320C5X.

C.1.8 SCRATCHPAD REGISTER (0xF007)

The scratchpad register is an 8-bit read/write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

C.1.9 INTERRUPT IDENTIFICATION REGISTER (0xF002)

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of Interrupt conditions are as follows:

1. Receiver line status (priority 1)
2. Received data ready (priority 2) or character time-out
3. Transmitter holding register empty (priority 3)
4. Modem status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt identification register (IIR). The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in the table below.

Table 6: INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET			
Bit 3	Bit 2	Bit 1	Bit 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	2	Received data available	Receiver data available	RBR Read
1	1	0	0	2	Character time-out indication	No characters have been received	RBR Read
0	0	1	0	3	THRE	THRE	IIR read or THRE write
0	0	0	0	4	Modem status	CTS, DSR, RI, or DCD	MSR read

IIR(0) can be used to indicate whether an interrupt is pending. When IIR(0) is low, an Interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in the table above.

IIR(3): This bit is always logic 0 when in the TL16C450 mode. This bit is set along with bit2 when in the FIFO mode and a trigger change level interrupt is pending.

IIR(4) - IIR(5): These two bits are always set to a logic 0.

IIR(6) - IIR(7): These two bits are always cleared in the TL16C450 mode. They are set when bit 0 of the FCR is set..

C.1.10 INTERRUPT ENABLE REGISTER (0xF001)

The interrupt enable register (IER) is used to independently enable the four serial channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by resetting IER(0) - IER(3) of the interrupt enable register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the interrupt identification register and the active (high) interrupt output. All other system functions operate in, their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are described below:

IER(0) Enable Received Data Available Interrupt

When set to one, IER(0) enables the received data available interrupt and the time-out interrupts in the FIFO mode.

IER(1) Enable Transmitter Holding Register Empty Interrupt

When set to one, IER(1) enables the transmitter holding register empty interrupt.

IER(2) Enable Receiver Line Status Interrupt

When set to one IER(2) enables the receiver line status interrupt.

IER(3) Enable Modem Status Interrupt

When set to one, IER(3) enables the modem status Interrupt.

IER(4) - IER(7).

These four bits of the IER are logic 0.

C.1.11 RECIEVER

Serial asynchronous data is input into the SIN pin. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN Input.

The Line Control Register determines the number of data bits in a character [LCR(0), LCR(1)]. If parity is used LCR(3) and the polarity of parity LCR(4) are needed. Status for the receiver is provided in the line status register. When a full character is received, including parity and stop bits, the data received indication in LSR(0) is set high. The CPU reads the receiver buffer register, which resets LSR(0). If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). If there is a parity error, the parity error is set in LSR(2). If a stop bit is not detected, a framing error indication is set in LSR(3).

If the data into SIN is a symmetrical square wave, the center of the data cells will occur with +/-3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 1 6X clock cycle prior to being detected.

C.1.12 MASTER RESET

After power up, the ACE Reset Input should be held low for one microsecond to reset the ACE circuits to an Idle mode until initialization. A low on RESET causes the following:

1 . Initializes the transmitter and receiver clock counters.

2. Clears the Line Status Register (LSR), except for the transmitter shift register empty(TEMT) and transmit holding register empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), divisor latches, receiver buffer register, and transmitter buffer register are not affected.

Following the removal of the reset condition (Reset high), the ACE remains in the idle mode until programmed.

A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the ACE is given in the table below.

Table 7: RESET

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt Enable Register	Master Reset	All bits low (0-3forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high. Bits 1,2,3,6,and 7 low,Bits 4-7 permanently low
Line Control Register	MasterResult	All bits low
Modem Control Register	Master Reset	All bits low
FIFO Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low,except 5 and 6 are high
Modem Status Register	Master Reset	Bits 0-3 low,bits 4-7 input signal
SOUT	Master Reset	High
Interrupt (RCVR errors)	Read LSFV/Reset	Low
Interrupt (RCVR data ready)	Read RBFV/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
OUT2-	Master Reset	High
RTS-	Master Reset	High
DTR-	Master Reset	High
OUT1-	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (MS&LS) Registers	Master Reset	No effect
Receive Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
RCVR FIFO	MR/FCR2-FCR0/ Change of FCR0	All bits low
XMIT FIFO	MR/FCR2-FCR0/ Change ofFCR0	All bits low

C.1.13 PROGRAMMING

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the Interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

FIFO Interrupt Mode Operation

The following RCVR status occurs when the RCVR FIFO and receiver Interrupts are enabled:

1. LSR(0) is set when a character is transferred from the shift register to the RCVR FIFO. When the FIFO is empty, It is reset.

2. IIR = 06 receiver line status interrupt has higher priority than the received data available Interrupt IIR = 04.

3. Receive data available interrupt will be issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level, it will be cleared.

4. IIR = 04 (receive data available indication) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following RCVR FIFO character time-out status occurs when RCVR FIFO and receiver interrupts are enabled.

1. If the following conditions exist, a FIFO character time-out interrupt occurs.

   – Minimum of one character in FIFO

   – Last received serial character was longer than 4 continuous previous character times ago (If two stop bits are programmed, the second one is included in the time delay).

– The last CPU read of the FIFO was more than 4 continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.

2. By using the RCLK input for a clock signal, the character times can be calculated. (The delay is proportional to the baud rate.)

3. The time-out timer is reset after the CPU reads the RCVR FIFO or after a new character is received, when there has been no time-out interrupt.

4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

XMIT Interrupts occur as follows when the transmitter and XMIT FIFO interrupts are enabled (FCR0 = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR = 02)occurs. The interrupt is cleared as soon as the transmitter holding register is written to or the IIR is read. One to sixteen characters may be written to the transmit FIFO when servicing this interrupt.

2. The XMIT FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following occurs:

THRE = 1 and there has not been a minimum of two bytes at the same time in XMIT FIFO, since the last THRE = 1. The first transmitter interrupt after changing FCR0 will be immediate, however, assuming it is enabled.

RCVR FIFO trigger level and character time-out interrupts have the same priority as the received data available interrupt. The transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty interrupt.

C.1.14 FIFO POLLED MODE OPERATION

Resetting IER0, IER1, IER2, IER3, or all to zero, with FCR0 = 1, puts the ACE into the FIFO polled mode. RCVR and XMITER are controlled separately. Therefore, either or both can be in the polled mode. In the FIFO polled mode there is no time-out condition indicated or trigger level reached. However, the RCVR and XMIT FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

Appendix D

TLC320AD55C Data Sheet

This appendix provides you with a description of the TLC32AD55C Sigma Delta Interface Circuit.

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D.0 Overview of the TLC320AD55C

The Texas Instruments TLC320AD55C provides high resolution low-speed conversion from digital-to analog (D/A) and from analog-to-digital(A/D) using oversampling sigma-delta technology. In this document this device may be referred to as the AIC or analog interface circuit. This device consists of two serial synchronous conversion channels (one input and the other output). It also includes an interpolation filter before the A/D converter and a decimation filter after the D/A converter. Other overhead functions provides are analog filtering, and on-chip timing and control. The sigma-delta architecture of the device produces high resolution, A/D and D/A conversions at low system speeds and low cost.

The AIC can be programmed through the serial interface to select options and circuit configurations. The options include reset, power down, communications protocol, serial clock rate, signal sampling rate, and the test mode. The circuit configurations may include a selection of input ports to the A/D converter, analog loopback, digital, loopback, decimator sinc filter output, decimator FIT filter finite-duration impulse-response (FIR) filter output, interpolator sinc filter output, and interpolator FIR filter output.

For a complete description of the device the read is referred to the Texas Instruments data sheet on this device, part #SLAS085

D.1 Key Features of the TLC320AD55C

The TLC320AD55C has the following features:

- 28 pin dual in line package (small outline)
- Requires only 5 volt power supply
- General purpose 16 bit signal processing
- 2s complement format
- Serial Port interface
- Minimum 80 dB harmonic distortion plus noise
- Differential architecture
- Internal reference voltage (Vref)
- Internal 64x oversampling
- Analog output with programmable gain(1, 1/2, 1/4, and 0)
- Phone mode output
- Variable conversion rate selected as MCLK/(Fk x 256), Fk=1,2...256
- System test modes (digital and analog loopback tests)

D.2 TLC320AD55C to DSP Interface

TLC320AD55C interfaces to the C5X DSP through the synchronous serial port. The 5 position jumper platform JP8 on the EVM320C5X is used to connect the serial port to the AIC. These 5 jumpers **must** be installed to connect the TLS320AD55C to the synchronous serial port of the DSP.

The analog input (INM or INP) is driven from either RCA Jack J2 and the analog output (OUTM or OUTP) is driven to RCA Jack J3.

D.3 Terms and Definitions

The following terms and definitions are used in the explanation of the functionality of this device:

Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and this data transfer is initiated by the falling edge of the frame-sync signal
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software control data
Primary Communications	The digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary Communications	The digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by the hardware or software.
Frame Sync	The falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals.
f_s	The sampling frequency that is the reciprocal of the sampling period.
Frame-sync Interval	The period occupied by 16 shift clocks. It goes high on the sixteenth rising edge of SCLK after the falling edge of the frame sync.

ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT.
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Dxx	A bit position in the primary data word (xx is the bit number).
DSxx	A bit position in the secondary data word (xx is the bit number).
d	The alpha character *d* is used to represent valid programmed or default data in the control register format (refer to secondary serial communications) when discussing other data portions of the register.
X	The alpha character *X* represents a don't-care bit position within the control register format.
FIR	Finite-duration impulse response.

D.4 Register Map

The AIC has six data and control registers. They are numbered 0 through 5 and their address is decoded in bits D8-D12 of the data. Data bit D13 determines a read or write cycle to the addressed register. When data bit D13 is low, a write cycle is generated. The table below shows the decoding.

Table 1: Register Mapping

Register #	D15	D14	D13	D12	D11	D10	D9	D8	Register Name
0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0	Control 2
3	0	0	0	0	0	0	1	1	Fk divide
4	0	0	0	0	0	1	0	0	Fsclk divide
5	0	0	0	0	0	1	0	1	Control 3

D.5 Register Functionality

The functionality of each register is defined by bits D0-D7. These functions are described below:

Register 0 The no operation (No-op) register. The 0 register allows secondary requests without any other register.

Register 1 The Control 1 register. The data in this register controls:

- The software reset (bit D7).
- The software power-down (bit D6).
- Selection of the normal or auxiliary analog inputs (bit D5).
- The output amplifier gain (1, 1/2, 1/4, or 0(squelch)) (bits D3, D4).
- Selection of the analog loopback (bit D2).
- Selection of the digital feedback (bit D1).
- 16-bit or 15-bit mode of operation (bit D0).

Table 2: Control Register 1 Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	-	-	-	-	-	-	-	Software reset
0	-	-	-	-	-	-	-	Software reset not asserted
-	1	-	-	-	-	-	-	Software power down (analog and filters)
-	0	-	-	-	-	-	-	Software power down not asserted
-	-	1	-	-	-	-	-	Select AUXP and AUXM
-	-	0	-	-	-	-	-	Select INP and INM
-	-	-	0	0	-	-	-	Analog output gain = 1
-	-	-	0	1	-	-	-	Analog output gain = 1/2
-	-	-	1	0	-	-	-	Analog output gain = 1/4
-	-	-	1	1	-	-	-	Analog output gain = 0 (squelch)
-	-	-	-	-	1	-	-	Analog loopback asserted
-	-	-	-	-	0	-	-	Analog loopback not asserted
-	-	-	-	-	-	1	-	Digital loopback asserted
-	-	-	-	-	-	0	-	Digital loopback not asserted
-	-	-	-	-	-	-	1	16-bit mode (hardware secondary requests)
-	-	-	-	-	-	-	0	Not 16-bit mode (software secondary requests)

The default register value for the Control 1 register is 00000000.

Register 2 The Control 2 register. The data in this register:

- Contains the output flag indicating a decimator FIR filter overflow (bit D5).
- Contains Flag 0 and Flag 1 output values for use in the phone mode (bit D3, D4).
- Selects the phone mode (bit D2).
- Selects or bypasses the decimation FIR filter (bit D1).
- Selects or bypasses the interpolator FIR filter (bit D0).

Table 3: Control Register 2 Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0	Function
X	X	-	-	-	-	-	-	Reserved
-	-	X	-	-	-	-	-	Decimator FIR overflow flag (valid only during read cycle)
-	-	-	X	-	-	-	-	FLAG 1 output value
-	-	-	-	X	-	-	-	FLAG 0 output value
-	-	-	-	-	1	-	-	Phone mode enabled
-	-	-	-	-	0	-	-	Phone mode disabled
-	-	-	-	-	-	1	-	Normal operation with decimator FIR filter
-	-	-	-	-	-	0	-	Bypass decimator FIR filter
-	-	-	-	-	-	-	1	Normal operation with interpolator FIR filter
-	-	-	-	-	-	-	0	Bypass interpolator FIR filter

The default register value for the Control 2 register is 00000000. The suggested values for the reserved bits is zero

Register 3 The Fk divide register. This register controls the filter clock rate and the sample period (bits D0-D7 = divide value).

Table 4: Fk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	Divide Value
1	1	1	1	1	1	1	1	255
				. . .				
1	0	0	0	0	0	0	0	128
				. . .				
0	0	1	0	0	0	0	0	32
				. . .				
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

The default register value for the Fk Divide register is 00001000. The oversampling clock (FCLK) is set as MCLK/(Fk x 4). MCLK/(Fk x 256) is the sample frequency (conversion rate) for the converter. when Fk is programmed to zero, its values is interpreted as 256.

Register 4 The Fsclk divide register. This register controls the shift (data) clock rate (bits D0-D7 = divide value).

Table 5: Fsclk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	Divide Value
1	1	1	1	1	1	1	1	255
				. . .				
1	0	0	0	0	0	0	0	128
				. . .				
0	0	1	0	0	0	0	0	32
				. . .				
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

The default register value for the Fsclk Divide register is 00001000. SCLK is set by MCLK/(2 x Fsclk). SCLK is for the serial transfer of data to and from the TLS320AD55C. When Fsclk is programmed to zero, its values is interpreted as 256.

Register 5 The Control 3 register. This register enables and disables the DAC reference (bit 3).

Table 6: Control Register 3 Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	0	1	0	0	0	DAC reference disabled
0	0	0	0	0	0	0	0	DAC reference enabled

D.6 TLC320AD55C Functional Description

D.6.1 Device Functions

The following sections describe the functions of the device

D.6.1.1 Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by the following equation:

f_s = Sampling (conversion) frequency = MLCK frequency/((Fk register value) x 256)

The inverse is the time between the falling edges of two successive primary frame-synchronization signals and it is the conversion period.

The input and output data clock (SCLK) is given by the following equation:

SCLK frequency = MCLK frequency /((Fsclk register value) x 2)

D.6.1.2 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data.

The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port, DOUT, during the frame-sync interval (one word for each primary communication interval). During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address, and the read bit (D13) set to 1. When a register read is requested, all 16 bits are 0 in the secondary word.

D.6.1.3 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host processor during the primary communications interval and latches the data on the 17th rising edge of SCLK. The data is converted to an analog voltage by the DAC and then passed through a (sin x)/x correction circuit and smoothing filter. An output buffer with three software-programmable gains (0 dB, -6 dB, and -12 dB) drives the differential outputs OUTP and OUTM. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data is read into the device control registers.

D.6.1.4 Serial Interface

The digital serial interface consists of a shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame synchronization interval, SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from the DOUT when the read bit (D13) is set to a 1. In addition, SCLK transfers control and device parameter information into DIN.

D.6.1.5 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the rising edge of the frame-sync signal. When the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the no-op register (register 0), and register programming does not take place during the communication.

DOUT is released from the high impedance state on the falling edge of the primary or secondary frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit D13 to a 1 in the addressed register. When the register is in the read mode, no data can be written to the register during this cycle. To return the register to the write mode requires a subsequent secondary communication.

D.6.1.6 Sigma-Delta ADC

The sigma-delta ADC is a fourth order, sigma-delta modulator with 64-times oversampling. The ADC provides high resolution, low noise performance using oversampling techniques.

D.6.1.7 Decimation Filter

The decimation filter reduces the digital filter rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a sixteen-bit, 2s complement data word clocking the sample rate.

NOTE:
The sample rate is determined through a programmable relationship of MCLK/(Fk x 256), Fk= 1,2,3...,256

D.6.1.8 Sigma-Delta DAC

The sigma-delta ADC is a fourth order, sigma-delta modulator with 64-times oversampling. The ADC provides high resolution, low noise performance from a one-bit converter using oversampling techniques.

D.6.1.9 Interpolation Filter

The interpolation filter samples the digital data at the rate of 64 times the incoming sample rate. The high speed data output from this filter is then used in the sigma-delta DAC.

D.6.1.10 Switched-Capacitor Filter

A switch-capacitor filter network is implemented on the analog output to provide a low pass operation with high rejection in the stop band.

D.6.1.11 Analog/Digital Loopback

The loopbacks provide a means of testing the ADC/DAC channels and can be used for in-circuit system level tests. The loopbacks feed the appropriate output back to the corresponding input on the device.

The test capabilities include an analog loopback between the two analog paths and a digital loopback between two digital paths. Each loopback is enabled by setting D1 or D2 in the Control 1 register.

D.6.1.12 DAC Voltage Reference Enable

The DAC voltage reference can be disabled through the Control 3 register. This allows the use of an external voltage reference applied to the DAC channel modulator. By supplying the external reference, the user can scale the output range of this channel. The internal reference value is 3.6 volts which provides a 6 volt peak-to-peak, differential output. The ratio of an external reference to the internal reference determines the output voltage range of the DAC channel as shown in the following equation:

$$V_{O(PP)} = V(\text{External Reference}) \times 6 \text{ volts} / 3.6$$

NOTE:

The distortion and noise specifications listed in the hardware specifications apply only under the following condition

$$V(\text{External Reference}) / 3.6 \leq 1$$

D.6.1.13 FIR Overflow Flag

The decimator FIR filter provides an overflow flag to Control 2 register to indicate that the input to the filter has exceeded the range of the internal filter calculations. When this bit is set in the register, it remains set until the register is read by the host. Reading this value always resets the overflow flag.

D6.2 Terminal Descriptions

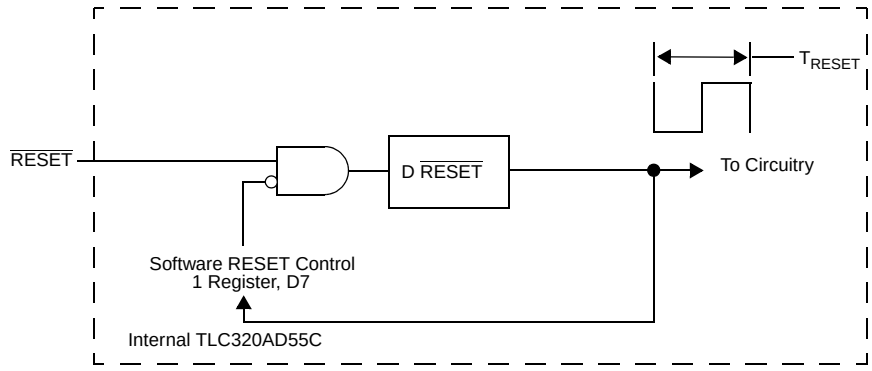
The following sections describe the terminal functions.

D.6.2.1 Reset and Power Down

The figure below shows the TLC320AD55C resets both the internal counters and registers, including the programmed registers in two ways;

- By applying a low-going reset pulse to the $\overline{\text{RESET}}$ terminal
- By writing to the programmable software reset bit (D7 in Control 1 register)

$\overline{\text{PWRDWN}}$ reset the counters only and preserves the programmed register contents. The DAC resets to the 15-bit mode.



Note: RESET- to circuitry is at least 6 MCLK periods long and releases on the positive edge of MCLK.

D.6.2.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are:

Counter reset - This signal resets all the flip-flops and latches that are not externally programmed, with the exception of those generating the reset pulse itself. Additionally, this signal resets the software power-down bit.

Counter reset = $\overline{\text{RESET}}$ terminal or reset bit or $\overline{\text{PWRDWN}}$ terminal.

Register reset - This signal resets all the flip-flops and latches that are not reset by the counter reset, except those generating the reset pulse itself.

Register reset = $\overline{\text{RESET}}$ terminal or reset bit.

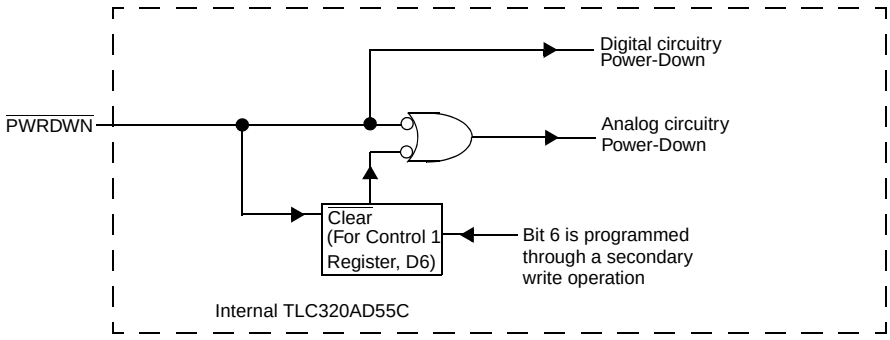
Both reset signals are at least six MCLK periods long (T_{RESET}) and release on the trailing edge of MCLK.

D.6.2.3 Software and Hardware Power-Down

Given the previous definitions, the software-programmed power-down condition is cleared by programming the software bit (Control 1 register, bit D6) to a 0 or is cleared by cycling the power on the device, bringing $\overline{\text{PWRDWN}}$ low, or bringing $\overline{\text{RESET}}$ low.

$\overline{\text{PWRDWN}}$ removes the power to the entire chip. The software-programmable, power-down bit only removes power from the analog section of the chip, which allows a software power-up function. Cycling the power-down terminal from high to low and back to high resets all the flip-flops and latches that are not external programmed, thereby preserving the register contents with the exception that the software power-down bit is cleared.

When $\overline{\text{PWRDWN}}$ is not being used, it should be tied high [V_{DD}(ADC) is preferred].



D.6.2.4 Master Clock Circuit

The master clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master clock input. SCLK is derived from MCLK [SCLK = MCLK/(Fsclk x 2), Fsclk = 1,2,3... 256] in order to provide clocking of the serial communications between the device and a DSP. The sample rate of the data paths is set as MCLK/(Fsclk x 256). Fk and Fsclk are programmable registers values used as divisors of MCLK. The default value for the Fk and Fsclk register is decimal 8.

D.6.2.5 Data Out (DOUT)

DOUT is taken from the high impedance state by the falling edge of the frame-sync. The most significant bit of data then appears on DOUT.

DOUT is placed in a high impedance state on the sixteenth rising edge of SCLK (internal or external) after the falling edge of the frame-sync signal. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/$\overline{W}$) bit with the eight MSBs set to zero. when a register read is not requested, the secondary word is all zeros

D.6.2.6 Data In (DIN)

In the primary communication, the data word is the input signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function.

D.6.2.7 Hardware Program Terminal (FC)

The input provides for hardware programming requests for secondary communication. It works in conjunction with the control bit D0 of the secondary data word. The signal on the FC is latched 1/2 shift clock after the rising edge of the next internally generated primary frame-sync interval. FC should be tied low when not being used.

D.6.2.8 Frame-Sync

The frame-sync signal indicates that the device is ready to send and receive data. The data transfer from DOUT and into DIN begins on the falling edge of the frame-sync signal.

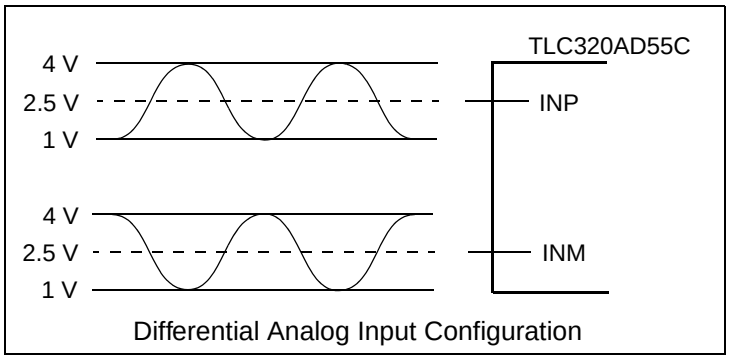
The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during the 16 bit transfer.

D6.2.9 Multiplexed Analog Input

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel.

D.6.2.10 Analog Input

The signal applied to the terminals INM and INP should be differential to preserve the device specifications. This is shown below. A single-ended input signal should always be converted to a differential input signal prior to being used by the TLS320AD55C. The signal source driving the analog inputs (INM, INP, AUXM, or AUXP) should have a low source-impedance for lowest noise performance and accuracy.

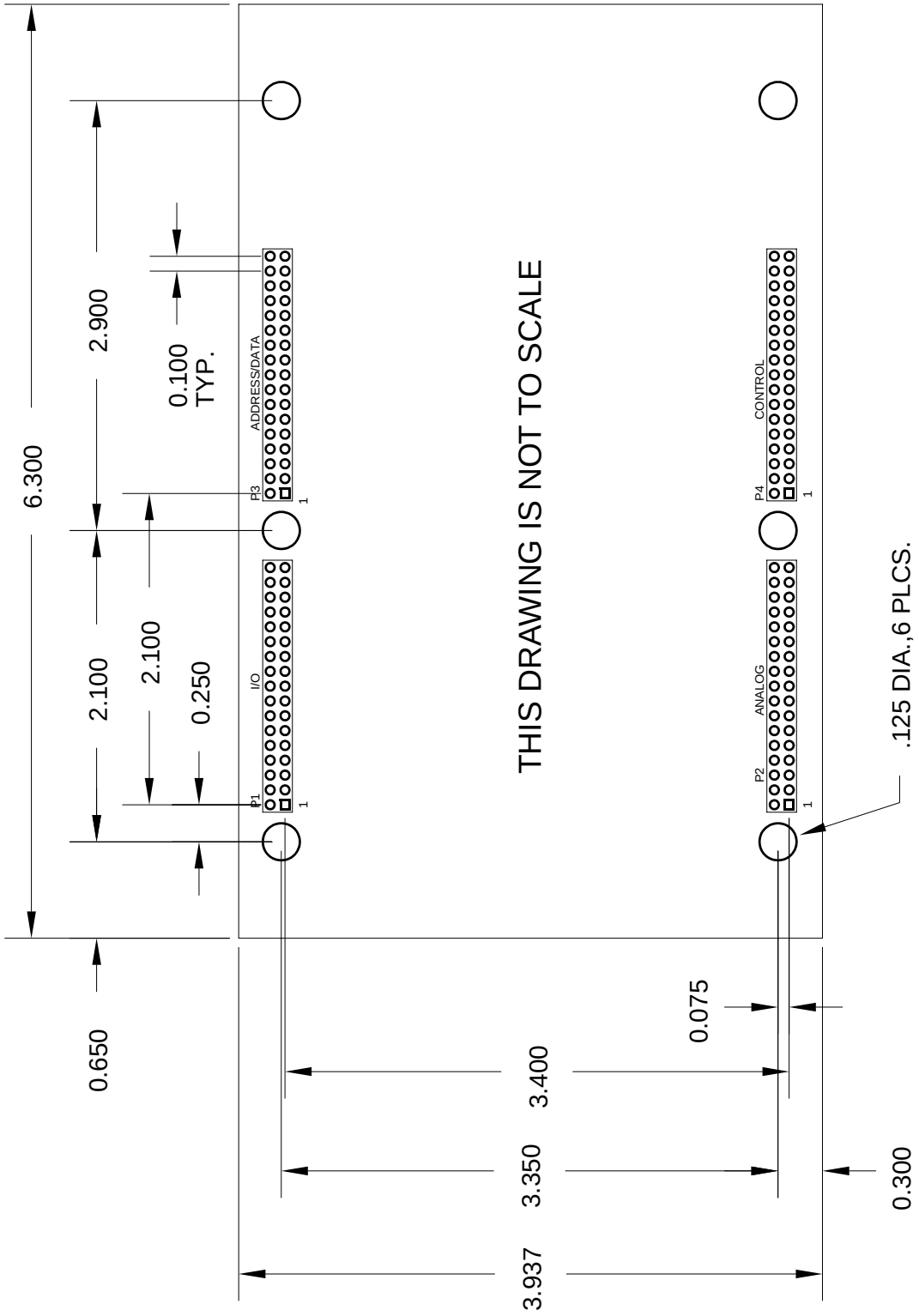


Differential Analog Input Configuration

Appendix E

EVM320 Mechanical Information

This appendix contains the mechanical information about the EVM and Wire Wrap Protoype Modules produced by Spectrum Digital.


THIS DRAWING IS NOT TO SCALE
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2.900
0.100
TYP.
2.100
2.100
0.250
0.650
0.075
3.400
3.350
3.937
0.300
.125 DIA.,6 PLCS.
P1
I/O
P2
ANALOG
P3
ADDRESS/DATA
P4
CONTROL

[redacted]

Printed in U.S.A., November 1997
503481-0001 Rev. B